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Front Pages

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Editorial and Reviewers' Board

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The current issue is the third of the eleventh volume of the *Athens Journal of Technology & Engineering (AJTE),* published by the Engineering & Architecture Division of ATINER.

Gregory T. Papanikos, President, ATINER.

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A World Association of Academics and Researchers

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- Abstract Submission: **19 November 2024**
- Acceptance of Abstract: 4 Weeks after Submission
- Submission of Paper: **26 May 2025**

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- Submission of Paper: **26 May 2024**

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- **Dr. Theodore Trafalis**, Director, Engineering & Architecture Division, ATINER, Professor of Industrial & Systems Engineering and Director, Optimization & Intelligent Systems Laboratory, The University of Oklahoma, USA.

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A Methodological Proposal for the Characterization of Building Heritage from the Second Twentieth Century for Renovation Purposes

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With the signing of the SECAPs, European cities and municipalities are taking steps to respond to an energy problem deriving from the demand for summer air conditioning, which, since the early 2000s, has exceeded the demand for winter heating. Sustainable urban regeneration requires action by applying an integrated approach between the sectors and professional figures involved, following the principles of sustainable development. Sustainable construction focuses on reducing the environmental impact of the building industry using renewable and recyclable materials, reducing energy consumption and embodied energy of building materials. The recycling and reusing of waste materials can lead to energy savings, cost reductions, potentially improved products, and reduced waste generation-related hazards to the environment. However, an important consideration when using green construction materials as alternative raw materials is having a thorough understanding of their chemical, mineralogical, and physical properties. This knowledge is essential to ensure that recycled materials can be effectively integrated into materials production without negatively impacting the final product quality or production efficiency. We present here processes developing existing materials which are substantial to ensure the maintenance of that heritage recognized, experienced and enjoyed by the people living a given territory.

Keywords: *global change, urban environment, building materials, building heritage and renovation*

Introduction

The building heritage of the Second Twentieth Century, although recognized as being of cultural interest by the urban planning instrument in force, remains at risk of tampering or demolition as the community of citizens, and particularly the

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properties, do not recognize its cultural value and identity. The main objective of this study is to design the possibility of intervention in this protected heritage, to increase the energy consumption mitigation and environmental adaptation character while respecting the architectural and stylistic language that distinguishes it.

The building restoration should ensure the structural and aesthetic integrity of the existing plasters to maintain their original appearance and chemical-physical characteristics. The mixture and color of the material used must be compatible with the existing ones, so it is necessary to identify an ideal mixture of plaster that does not differ from the original.

The Municipality of Bologna' Building Regulations, approved in the context of the General Urban Plan (PUG), in the "Approfondimenti conoscitivi" - Tavole dei Vincoli (and by the previous RUE in the "Disciplina dei materiali urbani" - art.57). Bologna General Urban Plan recognizes, among the existing building architectural Heritage, the "buildings of interest from the Second Half of the Twentieth Century" in order to take into consideration the material and cultural Heritage matured over the last century. The cataloging has divided the built Heritage of the Twentieth Century based on a chronological criterion: the manufacts built in the period between 1915 and 1949 have been collected in the category of buildings of historical-architectural interest of the Modern, the manufacts after 1949 made up the category of buildings of cultural and testimonial interest of the Second Half of the Twentieth Century. The criterion that led to considering only a few buildings from the last century was based on the classification previously made by the PSC and on the existence of files concerning the buildings drawn up by the MiC (Ministry of Cultural Heritage of Italy) and the IBC (Institute of Cultural Heritage of Italy), which decreed their architectural quality. Furthermore, the buildings restricted by the Superintendency were added after verifying that they had been built in the reference period. It should be noted that since the construction is recent, the danger of tampering and/or demolition is particularly high, as awareness and sensitivity in this regard is left to the owners, as a regulatory limit of intervention does not currently support them. Legislative Decree 42/2004 explicitly excludes from its protection works by living authors or whose execution does not go back more than fifty years (Article 10 paragraph 5), however it seems that it can be protected through the copyright law in as a work of art, but if this law protects a subjective right. It does not seem easily usable in the context of the public interest. It is a question of activating a reflection, also of a legal-regulatory type, as well as on the definition and delimitation of the objects to be protected, on the regulatory instruments to be put in place, possibly exploring new forms that the autonomy of the local authority. This Heritage is recognized but there is no cultural perception of its presence, nor of its cultural relevance, and there is the risk of losing part of it. In fact, in this period of major interventions on the building Heritage, which generally focuses on buildings dating from the 1960s up to today, there is the risk of proceeding with "not respectful" interventions only to increase energy performance in order to respond to mitigating needs of today's city.

To address this issue, we are conducting a study in the Bolognina District (Municipality of Bologna, Italy) an analysis of the materials of the exterior vertical

walls of one building identified as of interest from the Second Twentieth Century, characterized by plaster and tiles covering. The objective is to develop cooling materials that, in addition to ensuring higher reflectivity (albedo), can respect the style and architectural language while improving the indoor and outdoor well-being. Such new coatings will not inhibit but rather enhance the thermo-hygrometric exchange between indoor and outdoor, ensuring the physiological well-being of the individual. A methodology is proposed below for the application of new materials with the primary objective of increasing the energy and adaptation performance of the protected building heritage of the second half of the twentieth century, guaranteeing respect for the characterizing architectural/stylistic elements and stimulating the sensitivity of the community to regard. The cool materials were studied to guarantee the high reflexivity (albedo) that characterizes them, can respect the architectural style and language and improve the outdoor well-being of buildings, and improve, if not at least keep unchanged, the indoor one. About indoors, it is understood that these new vertical packages do not alter, but rather tend to improve the thermo-hygrometric exchange between indoor and outdoor environments, guaranteeing the physiological well-being of citizens, with particular attention to the weakest groups.

Materials and Methods

Ceramic Tiles Characterization

Ceramic tiles are building materials that can be easily modified to become solar reflective surfaces because of their high intrinsic thermal emissivity (ε = 0.90), excellent durability over time, and resistance to dirt and fouling due to a topcoat ceramic glaze. Another advantage of ceramic materials is the possibility of obtaining coloured products by ink-jet printing, allowing the fabrication of solar reflective ceramic materials with improved aesthetic characteristics (the so-called cool colours) (Cedillo-González et al. 2022, 2023). These materials present a coloured response in the visible wavelength range and higher SR values than conventional materials of the same colour. Moreover, ink-jet-derived solar reflective tiles increase customization capabilities, making it possible to restore historical buildings without compromising their architectural value.

Conventional solar reflective products are constituted by a support, a reflective basecoat, and an IR-transparent topcoat to protect the basecoat. This configuration recalls the layout of porcelain stoneware tiles, which are fabricated by a layer configuration: the ceramic support (1st layer), the engobe (2nd layer), the digital colouration (3rd layer), and the glaze (4th layer). Following this premise, several authors have designed ceramic tiles with high solar reflectance. For instance, Ferrari et al. (2013) designed glazed ceramic tiles with high solar reflectance (SR = 0.90) by adding $ZrSiO_4$ and TiO_2 to the engobe's formulation. As authors found that the ceramic engobe plays a crucial role in enhancing the solar reflective properties of tiles, Governatori et al. (2021) focused their attention on designing high-reflectance glass-ceramic frits, which are a critical component of the

engobe's formulation. In a second work, the same authors investigated the obtainment of solar-reflective ceramic tiles by modifying the engobe's formulation, finding that when a glass-ceramic frit with a high intrinsic SR value is incorporated into the formulation of an industrial engobe, it can raise its albedo (Governatori et al. 2022).

An additional advantage of developing white and coloured solar reflective porcelain stoneware ceramic tiles is that their production allows the incorporation of secondary raw materials (SRMs) in all of their elements: support, engobe and glaze. The use of SRM will lead to additional energy savings during the production process and a reduction of the environmental impact of the final products. However, it is known that ink-jet decoration negatively affects the albedo of tiles prepared with reflective engobes due to its coverage by the inks and their mineralogical composition (Cedillo-González et al. 2022, 2023). For this reason, the albedo of the engobe should be as high as possible to compensate for this reduction by ink-jet decoration. This work produced a set of functional solar reflective engobes using several SRMs such as recycled glasses (four types), chamotte, granite waste, and waste yttria-stabilized zirconia from term spraying processes. The obtained engobes were characterized by CIELab colour (colorimetric model), gloss, optical dilatometry and solar reflectance. Their properties were compared with a conventional engobe of similar chemical composition.

The preparation of functional solar reflective engobes was investigated in three steps using several SRMs such as recycled glasses (photovoltaic glass, screen glass, and two types of urban-derived recycled glass), chamotte, granite waste, and waste yttria-stabilized zirconia (YSZ) from thermal-spraying processes. This study aimed to develop an engobe formulation with enhanced SR property, containing at least 30 wt. % of SRM. First, we conducted a preliminary study where a conventional frit-containing engobe (labelled here as "ESTD") made of conventional raw materials (RM) was modified by replacing 100% of the frit with several types of recycled glass. Additionally, 100% of the quartz and the K feldspar were substituted by chamotte and granite waste, respectively. The second step consisted of the modification of the previous engobe's formulations to reduce as much as possible the total molar content of TiO_2 and Fe_2O_3, as these oxides promote the development of yellow colouration, negatively affecting the SR property. Modifications were performed only for two formulations (as the others were already set at the minimum possible TiO_2 and Fe_2O_3 content) using the software Glaze Master® (Expert System Solutions, Modena, Italy). The third step consisted of adding 5 wt.% or 10 wt.% of a whitening agent in the engobe's formulations that presented the best colour (L^* = brightness), high SR property, and an adequate content of SRM. The aim was to further enhance the SR in anticipation of a reduction of this property when the ink-jet inks cover the engobe during the production of porcelain stoneware tiles (support + engobe + ink-jet decoration + glaze). The whitening agent is an SRM composed of waste YSZ from thermal-spraying processes. Here, the formulations of two selected engobes (those with the best properties) are presented in Table 1, where the number in the formulation's name represents the molar % of TiO_2 and Fe_2O_3 (the sum of the two

oxides) that was reduced. The number after the term "Zr" in the formulation's name represents the wt. % of waste YSZ that was added.

Table 1. *Formulations (Expressed as wt.%) of the Selected Functional Solar Reflective Engobes*

RM or SRM	ESTD	EGW27Zr10 (Formulation 1)	EMG14Zr5 (Formulation 2)
Na feldspar	20.00	18.17	41.65
K feldspar	20.00	-	-
Clay 1	15.00	-	-
Whitening 1	8.00	3.91	6.05
Clay 2	7.00	-	7.93
Kaolin	14.00	31.96	22.99
Whitening 2	8.00	7.33	7.92
Quartz	4.00	0.82	0.78
Frit	4.00	4.75	-
Granite waste	-	23.05	5.04
Mixed glass	-	-	2.63
Waste YSZ	-	10.00	5.00

All engobes were prepared according to a standard laboratory protocol. For each formulation, a mixture of 200 g of dry raw and secondary raw materials was placed in a 300 mL porcelain jar, along with 250 g of sintered alumina grinding bodies, 0.3 g of tripolyphosphate, 0.3 g of slurry modifier, and 84 g of tap water. A rapid mill was used to create a consistent slurry from the mixture, with a milling duration of 40 minutes. Two types of specimens were prepared: engobed porcelain stoneware tiles and 40 mm (Ø)-disks of pure engobes. The engobed tiles were used to measure the solar reflectance, gloss and colour (CIELab) properties of the engobes, while the disks-shaped specimens were useful to determine the thermal expansion coefficient ($\boldsymbol{\alpha}$) by optical dilatometry and the shrinkage. To prepare the engobed tiles, the density of the slurry was measured using a 100 mL steel pycnometer and adjusted to a value of 1.65 g/ml. The slurry was then precisely deposited on conventional and fired porcelain stoneware substrate, humidified using an airbrush, with a 0.6mm engobe thickness. The engobed tiles were fired in an industrial kiln utilizing a 50-min cold-to-cold firing cycle suitable for porcelain stoneware, with a maximum temperature of 1205 °C. The remaining mixture was dried at 110 °C for 12 h and ground with a porcelain mortar. The powdered engobes were humidified to 6 wt. % in a closed system for at least 24 h and then pressed at 30 bar to obtain the disk-shaped pressed specimens. After drying at 110 °C for 1 h, the pressed engobes were thermally treated in a laboratory furnace at 10 °C/min up to 1205 °C. An isotherm of 10 min was performed, and the engobes were naturally cooled inside the furnace. The shrinkage of the fired-pressed engobes was measured using a calliper with 0.01 mm resolution.

The brightness parameter (L^*) is a significant value that can be related to the SR property: high values usually correspond to high SR. Figure 1 presents the solar reflectance spectra of the selected engobes (3 specimens were measured) from which the solar reflectance (SR) values (presented in Table 2) were calculated.

Figure 1. *Solar Reflectance Spectra of the Selected Engobes from which the Solar Reflectance (SR) Values Were Calculated. (a) Formulation 1 (EGW27Zr10). (b) Formulation 2 (EMG14Zr5)*

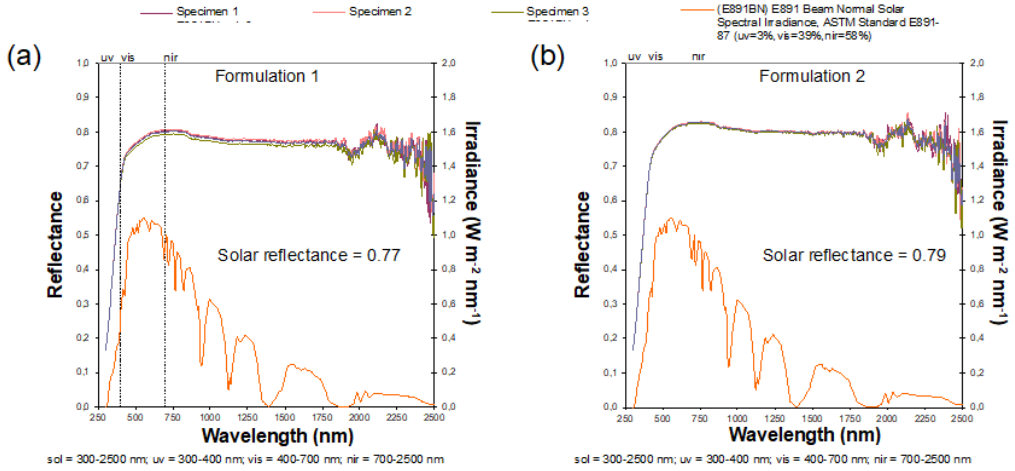


Table 2. *Technological and Aesthetic Properties of the Standard and Selected Engobes*

Formulation	% SRM	Shrinkage (%)	$\alpha/1 \times 10^7$	Gloss (60°)	Colour			SR
					*L**	*a**	*b**	
ESTD	0.0	9.52 ± 0.01	41.36	2.50 ± 0.00	89.3 ± 0.1	0.39 ± 0.04	5.58 ± 0.04	0.769 ± 0.001
Formulation 1	33.1	8.8 ± 0.2	44.15	2.43 ± 0.06	89.7 ± 0.3	0.13 ± 0.04	2.18 ± 0.07	0.771 ± 0.007
Formulation 2	12.7	8.65 ± 0.09	45.11	2.40 ± 0.00	88.9 ± 0.3	0.61 ± 0.02	5.09 ± 0.05	0.794 ± 0.002

The selected engobe formulations with reduced molar % of TiO_2 and Fe_2O_3 and containing 5 and 10 wt. % of the SRM waste YSZ (EGW27Zr10 and EMG14Zr5) present a slightly higher solar reflectance than the standard engobe. This reduced increase in the SR property is likely due to the use of SRM, which intrinsically contains some impurities in their chemical compositions, and those impurities can act as solar radiation absorbers in the final material. Additionally, it is worth mentioning that these formulations can be further improved to increase both the SR and the wt.% of SRM, as the conventional whitening agent and the zirconia raw materials can be further replaced using waste YSZ.

Table 2 presents a selection of the most significant technological and aesthetic properties of the engobes produced in this work. Shrinkage and thermal expansion properties are essential to setting the proper firing conditions for porcelain stoneware tiles. The materials' thermal properties should be compatible with ceramic support and the glaze to avoid deformation or crack formation. On the other hand, gloss and colour are two essential properties that increase the possibilities of industrial application and commercialization of the produced engobes in zero environmental impact buildings and constructions. Notably, in the era of ceramic ink-jet printing, high-quality decorations require engobes with high whiteness and opacity to allow the advantages of ink-jet decoration: the modification in real-time of the decoration patterns, the use of shorter times to change drawings and colours, the opportunity to perform easier testing at lower

costs, the increased ability of customization options, the possibility to perform edge-to-edge prints or decorate relief surfaces and a drastic reduction of the amounts of inks compared with the quantities used by traditional decoration systems (Cedillo-González et al. 2022). Table 2 shows that most of the selected engobes present a lower shrinkage value than the standard engobe. The engobes' thermal expansion coefficient ($\boldsymbol{\alpha}$) in the 50 °C – 400 °C interval was measured using the pressed samples. It was found that the produced engobes present $\boldsymbol{\alpha}$ values comparable to that of the standard engobe. The gloss of the engobes was measured on the fired tiles. It is worth noticing that incorporating several SRMs in the engobe formulation does not significantly affect the opacity of the engobes, as the samples presented gloss values comparable to those presented by the standard engobe. The colour was also measured on the fired tiles using the CIELab colour space. As in the case of gloss, incorporating several SRM in the engobe formulation does not significantly affect the colour of the engobes, as most of the samples present L^*, a^* and b^* values comparable to those presented by the standard engobe. Therefore, from the previous results, an important conclusion was derived: an urban-derived mixed recycled glass, granite waste and waste YSZ can be used to modify industrial ceramic engobes formulated with conventional RM without losing the aesthetic characteristics of the engobe.

Built Environment Characterization

The building under study (44°30’50.9” N, 11°20’49.7” E) was the former neighbourhood library (Biblioteca Pelagalli), then nursery school until 2012 – current headquarters of Hex, a coworking association, privately owned and was designed in the year ‘70 by the Architect designer Lorenzino Cremonini (1939-2014) (Figure 2). A microclimate and fluid dynamics analysis of the current context carried out with the ENVImet model during a day characterized by a heat wave, to understand the vulnerabilities present in the vicinity of the building under study. ENVI-met is a three-dimensional non-hydrostatic microclimate model designed to simulate the surface-plant-air interactions within daily cycles in the urban environment with a typical resolution of 0.5 to 10 m in space and 10 sec in time. Several variables can be simulated, included flow around and between building, exchange processes of heat and vapor at the ground surface and at the walls, turbulence exchanges, vegetation parameters, bioclimatology and particle dispersion (ENVI-met, Bruse and Fleer 1998).

Figure 2. *Architect Lorenzino Cremonini (Private Collection)*

A collection of data regarding the construction methods and previous interventions on the historic building and a survey in situ to collect samplings of the coatings (ceramic tiles and plaster) of the vertical masonry packages have been performed. Subsequently, a chemical analysis and mineralogical characterization of the collected material that makes up the package, with particular attention to the external coating was conducted by University of Modena and Reggio Emilia and CERTIMAC.

The new type of coating was studied to guarantee high reflectivity (cool material) and a good response to urban air pollution, even at this stage of the study limited to an increase of 10% of the surface albedo property. Thus, the new building project was characterized by an external vertical cladding made of ceramic tiles highly performing both in terms of reflectivity, sustainability, and resistance to atmospheric pollution.

A microclimate and fluid dynamics analysis of the project status of the building with the ENVImet model, with 1x1 m^2 horizontal resolution, has been conducted to assess in detail the foreseen effects of the new materials.

Figure 3 reports the actual configuration and condition of the investigated building. It is possible to note that the structure has a public or private commercial destination, but not as residential housing. As previously described, the construction period will see in the housing policies of the city of Bologna the need to combine the availability of housing with that of the development of buildings that act as a point of aggregation and socialization of the population.

This building, due to its particular architectural composition, was the object of admiration or strong criticism in those years, because it inserted a strong innovative drive into the city landscape by drawing on other European

experiences. This was not an isolated episode, with the passage of time also in other places (for example Milan, Italy) this new building method became increasingly established, and today it constitutes a large part of the cultural heritage of the entire nation's buildings.

Figure 3. *The Former Neighbourhood Library (Biblioteca Pelagalli), then Nursery School until 2012 – Current Headquarters of Hex, a Coworking Association, Privately Owned*

Table 3 reports the model input data of physical properties for the real tiles (Ex Ante, EA), the simulation performed by changing only the albedo values of tiles incrementing it by a 10% (Ex Post only Albedo, EPA), and the input data of the expected physical characteristics of the new tiles also incremented of 10% in the albedo values and imposed the new emissivity values at 0.90 for all the tiles of various colours (Ex Post Potential, PEP).

This numerical experiment was conducted to verify whether the modification of the albedo alone, which could be carried out with a mere surface treatment, can lead to differences of significant value for the surface temperature, or whether deeper modifications to the structure of the tiles are essential to obtain the desired effects.

Table 3. *Physical Properties Characterizing the External Walls of Biblioteca Pelagalli for Ex Ante (EA), Ex Post Only Albedo (EPA), and Potential Ex Post (PEP) Configurations*

EA	Red	Yellow	Orange	Green	Blue	White
Absorption (shortwave)	0.575	0.420	0.510	0.680	0.800	0.236
Reflection (shortwave)	0.425	0.580	0.490	0.320	0.200	0.764
Emissivity	0.906	0.889	0.900	0.887	0.906	0.879

Specific heat [J/(kg*K)]	770	770	770	770	770	770
Thermal conductivity [W/(m*K)]	1.072	1.072	1.072	1.072	1.072	1.072
Density [kg/m3]	2277.30005	2169.89990	2207.30005	2070.89990	2284.00000	2198.89990
EPA	**Red**	**Yellow**	**Orange**	**Green**	**Blue**	**White**
Absorption (shortwave)	0.532	0.360	0.460	0.640	0.770	0.160
Reflection (shortwave)	0.468	0.640	0.540	0.360	0.230	0.840
Emissivity	0.906	0.889	0.900	0.887	0.906	0.879
Specific heat [J/(kg*K)]	770	770	770	770	770	770
Thermal conductivity [W/(m*K)]	1.072	1.072	1.072	1.072	1.072	1.072
Density [kg/m3]	2277.30005	2169.89990	2207.30005	2070.89990	2284.00000	2198.89990
PEP	**Red**	**Yellow**	**Orange**	**Green**	**Blue**	**White**
Absorption (shortwave)	0.532	0.360	0.460	0.640	0.770	0.160
Reflection (shortwave)	0.468	0.640	0.540	0.360	0.230	0.840
Emissivity	0.900	0.900	0.900	0.900	0.900	0.900
Specific heat [J/(kg*K)]	600	600	600	600	600	600
Thermal conductivity [W/(m*K)]	1.100	1.100	1.100	1.100	1.100	1.100
Density [kg/m3]	2250	2250	2250	2250	2250	2250

Results and Discussion

The building was represented, in the three cases (EA, EPA, PEP) (EA), without the buildings actually present in its surroundings in order to see the maximum effect of the albedo variation. It was decided to maintain the vegetation close to the north façade in order to verify its possible influence. The most detailed cell resolution in ENVI-met is 1x1 m^2. Because of the complex chromatic design developed with the tiles that characterizes the building's facades, a simplification was necessary also to represents all the colours present in each single façade.

In Table 4 are reported the values of the wall temperatures obtained in EA, EPA, and PEP simulations for each colour tile in south façades. In the specific case of our simulation, a wish-list was adopted on the physical properties of the materials which unified the density values at 2250 kg/m^3 and increased the thermal conductivity for all from 1,072 to 1,100 W/mK. Furthermore, the emissivity values were standardized to 0.9.

Table 4. *Outside Wall Temperature Values Obtained by Envi-met Simulation for Ex Ante, ex post Only Albedo, and Potential Ex Post Scenarios for Each Colored Tile*

Hour	Parameter	Facade and color tile	EA	EPA	Comparison EA-EPA	PEP	Comparison EA-PEP
2:00 p.m.	T wall outside	Sud-blue (1)	61.71 °C	60.74 °C	- 0.97 °C	64.29 °C	2.58 °C
2:00 p.m.	T wall outside	Sud-blue (2)	58.32 °C	57.41 °C	-0.91 °C	60.58 °C	2.25 °C
2:00 p.m.	T wall outside	Sud-white (3)	40.78 °C	38.41 °C	-2.37 °C	39.19 °C	-1.59 °C
2:00 p.m.	T wall outside	Sud-white (4)	45.10 °C	42.61 °C	-2.49 °C	43.89 °C	-1.21 °C
2:00 p.m.	T wall outside	Sud-green (5)	56.74 °C	56.64 °C	-0.10 °C	56.80 °C	0.06 °C
2:00 p.m.	T wall outside	Sud-red (6)	53.55 °C	52.22 °C	-1.33 °C	54.78 °C	1.22 °C
2:00 p.m.	T wall outside	Sud-orange (7)	49.99 °C	48.49 °C	-1.50 °C	50.23 °C	0.24 °C

While maintaining the same structural characteristics for the tiles, and changing only the albedo increasing it by 10%, the decrease in the surface temperatures is well evidenced for all the various colours, for the simulation where the physical properties were changed a very different behaviour have been obtained.

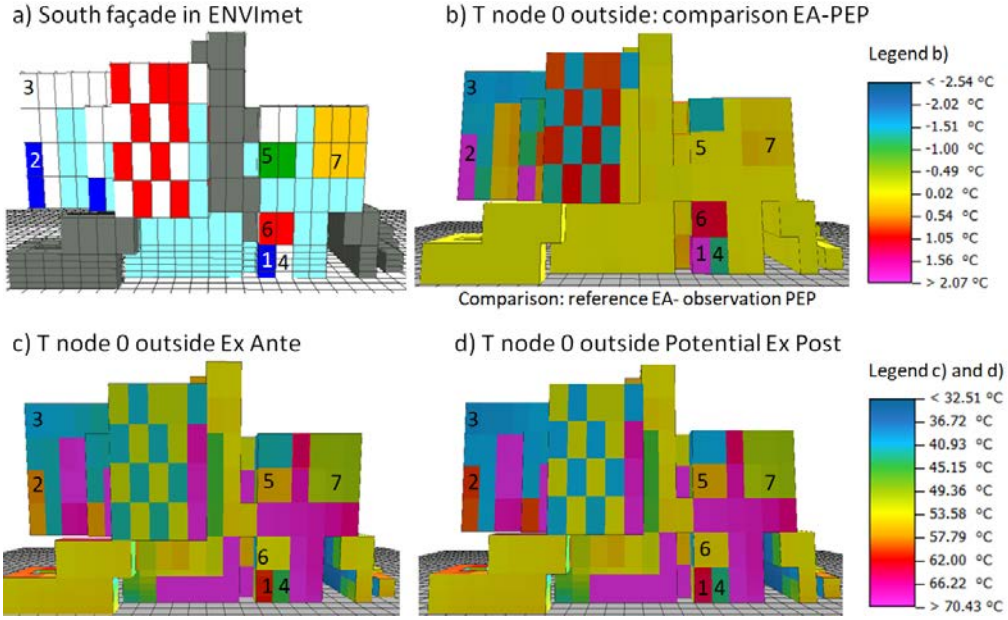
The outside wall temperature of improved blue tile at 2 p.m. shows a higher surface temperature (up to 2.58 °C). This can be explained throughout Figure 4 that shows that the tile 1 is very close to the surface so, probably, it is influenced by the radiant temperature emitted by the floor. The other blue tile (2 at 6m height) shows an increment of 2.25°C.

The white tile is the only one that shows an effective cooling of the wall of about -1.59°C near the walking surface and -1.21 °C at about 11 m height. The green tile does not show differences in the wall temperature (0.06 °C) while the red tile shows a warming of the wall surface (1.22 °C).

Some of these results for EA and PEP comparison appear to be counterfactual, that is, the current result appears to conflict with what was reasonably expected. In Figure 4 is reported the complexity of the facade in terms of tile colouring is reported. However, in our modelling simplification we have included the characteristics on the ground coverage and, therefore, the simulation is also

affected by this contribution, which differs at different heights of the building. This turns out to be a confounding effect on the results which would require an analysis in the laboratory, in controlled conditions, a turning point developed tiles trying to magnify the effects without however exceeding in the performances the current limitations foreseen by the urban regulations, such as for example those linked to potential glare effects at the street level. Thus, the evaluation work is still ongoing in parallel to the lab development of the new materials and will be followed through other deliverables within ECOSISTER Programme. From the same case study, the ageing effects of the ceramic tiles will be evaluated, to aid advising the industrial production on increasing materials resilience for weathering and air pollution in an urban context.

Figure 4. *Composition of the South Façade of the Building (a) and the Outside Wall Temperature Obtained by the Model for EA (c) and PEP (d) Simulations Along with their Comparison (b)*



What clearly emerges from the simulation is that the renovation of the tiles in buildings belonging to the cultural heritage needs detailed studies on the structural composition of the materials, as their physical properties, if not carefully calibrated, can give rise to effects that conflict with the desired results.

Conclusions

From the comparison made, the thermal excursion of PEP tiles in the temperature on the facade leads to a range of approximately 4.5 °C. The change in the albedo of the material can influence the thermal regime of the building but is not possible to evidence an effect on the well-being outdoor, except for possible glare phenomena which can cause high albedo values of the surfaces, including walls. Furthermore, it was found that the variation of the albedo alone produces

very small effects already at a superficial level and, therefore, significant effects on the outdoor environment is reasonable to exclude, even possible research developments may concern new simulations in ENVI-met gradually increasing the albedo to understand the most performing threshold values for each colour, to be able to give indications to the production sector.

At present, utilising the simulated values for the potential new tiles a limitation to only 10% in the albedo value it is debatable it can influence significantly the outdoor environment, as other authors already pointed out, even more studies are necessary to understand if the internal building energy consumption will be positively affected by the innovation (Fabbri et al. 2020, Lopez-Cabeza et al. 2022). As Lee and Mayer (2018) clearly outlined, higher albedo of the building walls causes an increase of mean air temperature and mean irradiance temperature, influencing the PET (Physiologically Equivalent Temperature) values, thus reflecting in a certain decrease of outdoor comfort (Matzarakis et al. 1999). While the increase in indoor thermal comfort is uncontroversial, the effects on the outdoor thermal values has to be specifically investigated case by case.

In our modelling experiment, some limitations to the performed modelling study are due to the oversimplification of the external fabric texture (i.e. surrounding buildings and pavements). As reported in Fabbri et al. (2020), the role of paved surfaces has a much more relevant influence on external comfort compared to the one due to the facades. However, the latter must be part of an overall review of the entire urban regeneration system, because it can provide a contribution, even if limited but, above all, it can contribute to preserving the identity of the places and the value system of the cultural heritage of the resident population.

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Self-locking Domino Logic Pipelined Controller for RISC-V in FPGA

By Florian Deeg[*], Xiangyuan Wu[±] & Sebastian M. Sattler[°]

This paper proposes an asynchronous RISC-V CPU design based on self-locking domino logic. The asynchronous approach offers advantages over traditional synchronous designs, including improved performance, lower power consumption, and greater modularity. The paper details the design and implementation of the asynchronous control unit using domino logic on an FPGA development board. The control unit is designed for a Turing-complete 32-bit RISC-V architecture. A significant aspect of the design is the self-locking mechanism, which ensures that the circuit only unlocks after all processing stages have been completed. This eliminates the need for a global clock and simplifies hazard-free operation. Furthermore, the paper discusses the potential for parallelizing the ALU using domino logic to improve performance further. The implementation of the asynchronous CPU has been analyzed in terms of power, performance, and area using the Vivado Design Suite. The power analysis indicates that the asynchronous processor consumes considerably less power in the clock network compared to its synchronous counterpart, thereby underscoring its energy efficiency. A performance analysis using the SPECint2000 benchmark suite demonstrates a 10% increase in performance, while only using slightly more area. These findings illustrate the asynchronous processor's potential for performance-critical applications while maintaining energy and area efficiency.

Keywords: *domino logic, asynchronous design, self-locking, RISC-V, GALS*

Introduction

Synchronous circuits represent the state of the art in circuit design. Still, asynchronous circuits are becoming increasingly important as they offer numerous advantages over synchronous circuits (performance, power consumption, modularity, no single-point-of-failure, no clock skew, etc.) (Sparsø 2001). Asynchronous circuits are also more resilient to fluctuations in the supply voltage and temperature. Local faults in asynchronous designs are often limited to the affected area, which increases fault tolerance. Furthermore, they generate less electromagnetic interference and are therefore more suitable for applications in which electromagnetic compatibility (EMC) plays an important role (Bouesse et al. 2007). However, the advantages of this approach are also offset by disadvantages, including the necessity for more complex design methods and an associated lack of design tools.

Field Programmable Gate Arrays (FPGAs) are a special hardware component distinguished by their high performance, flexibility, and energy efficiency. In

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contrast to conventional integrated circuits (ICs), which are pre-programmed for a specific function, FPGAs can be reconfigured after manufacture to undertake new tasks or optimize performance. This feature renders them an optimal platform for the development of demanding applications that require high computing power, low latency, and customizability.

For a considerable period, the market for processors was divided between two architectures: x86 and ARM, which are mainly used in mobile devices. In recent years, however, a new player has joined them and is providing a breath of fresh air in the form of RISC-V. RISC-V is a license-free instruction set architecture (ISA) that originated at the University of California, Berkeley (Waterman 2016). In contrast to x86, which has grown historically and is complex, RISC-V was developed from scratch. The principle of simplicity was prioritized. This simplicity is intended to minimize hardware costs on the one hand and increase flexibility on the other. RISC-V is becoming increasingly important in the processor world. One decisive factor is that it is license-free. This enables various companies and research groups to develop and utilize processors based on RISC-V. This has led to a wide variety of RISC-V processors that are used in different areas. The spectrum ranges from energy-efficient devices in the Internet of Things (IoT) to high-performance computers. Although RISC-V has not yet reached the market share of x86 and ARM, its growth potential should not be underestimated. The simplicity, flexibility, and license-free nature of RISC-V make it an attractive option for many developers. Other positive aspects of RISC-V include its energy efficiency, scalability, and security, as the basic architecture of RISC-V is so simple and offers little scope for attack.

Structure of the Paper

A brief literature review is conducted to distinguish this paper from others in the field. The following section presents the circuit structure, which comprises the self-locking pulse circuit, the dual-rail domino logic circuit, and the entire pipeline with completion detection and its realization in the FPGA. Subsequently, an existing synchronous multicycle RISC-V processor is briefly introduced, after which a control automaton for this Turing-complete processor is realized as a domino logic pipeline. It demonstrates how the pipeline can be utilized to control a globally asynchronous locally synchronous (GALS) system that can be arbitrarily divided into subcircuits to achieve the highest possible speed and safety. The subsequent chapter deals with the results and a comparison with synchronous automata. Finally, a conclusion and future work are presented.

Related Work

Dooply and Yun (1999) presented a method for optimizing clocking in self-resetting domino pipelines. This method employs soft synchronizers and roadblocks to allow time borrowing, thereby maximizing throughput and eliminating latch

overhead. The authors introduced a high-performance clocking methodology for self-resetting domino pipelines that optimizes the clock rate through time borrowing and robust handling of clock skew while eliminating latch overhead. However, their approach does not adequately simplify the complex clocking and synchronization management or provide a robust precharge management system, nor does it adequately simplify the complex clocking and synchronization management or provide a streamlined implementation and testing methodology. Jung et al. (2002) presented a high-speed add-compare-select (ACS) unit for Viterbi decoders using locally self-resetting CMOS (SRCMOS), which achieves significantly higher data rates compared to static and domino CMOS designs. This approach is associated with higher power consumption and increased design complexity due to the need for careful device sizing and additional components. In contrast, Jung et al. (2003) introduced a dual keeper structure and delay logic gates to enhance the performance and noise margin of domino logic gates, ensuring high-speed switching and robustness to noise and timing variations. However, their approach introduces additional design complexity and lacks a focus on scalability issues

In (Litvin and Mourad 2005) they presented the development of dual-rail self-resetting logic gates with input disable (DRSRLID) for fast and power-efficient arithmetic operations. They also demonstrated the application of these gates in a 16-bit parallel adder. However, their work primarily focuses on arithmetic circuits and does not extensively validate the logic in broader applications or address implementation complexity.

Alsharqawi and Einioui (2006) proposed two novel synchronization approaches for clockless pipelining of coarse-grain datapaths using self-resetting stage logic (SRSL) to achieve high throughput. The approach suffers from scalability issues and increased implementation complexity. Ramadass et al. (2014) introduced the Self Resetting Logic with Gate Diffusion Input (SRLGDI) technique to create low-power, high-speed logic circuits and demonstrated its effectiveness through the design and simulation of various adders. However, their approach increases transistor count and design complexity. The method of designing high throughput and ultra-low power asynchronous domino logic pipelines based on a constructed critical data path was introduced in (Xia et al. 2015). However, their approach does not fully address the challenges of design automation, placement, routing optimization, and timing verification. The implementation of low-power and high-performance asynchronous dual-rail interconnect using domino logic gates in 16-nm technology was proposed in (Rezaei and Moghaddam 2016). The integration of self-locking mechanisms or the detailed implementation of a complete RISC-V pipeline controller remains an issue. Sokolov et al. (2020) introduced a novel framework for automating the design of asynchronous logic control in AMS electronics, integrating formal verification and specialized analog-to-asynchronous interface components for handling non-persistent signals. It does not fully address the challenges of comprehensive design automation and efficient handling of nonpersistent signals within the FPGA implementation. Li et al. (2021) presents a methodology for implementing asynchronous phase-decoupled circuits using traditional electronic design automation (EDA) tools. The authors present an

asynchronous RISC-V processor implemented on the Xilinx ZCU102 FPGA, achieving a threefold improvement in dynamic power efficiency compared to its synchronous counterpart, while maintaining similar resource utilization. The approach demonstrates the potential of asynchronous design in reducing power consumption for IoT and neuromorphic applications, despite challenges in commercial tool support.

This work builds on the work in (Deeg and Sattler 2024), which focused on structural feasibility in the FPGA. In this paper, the design of the automaton and in particular the low-level design is described in more detail, with results of the asynchronous implementation.

Self-locking Domino Logic

This section presents the structure and realization of the self-locking domino logic in the FPGA. The delay-insensitive domino logic was selected to minimize constraints in the design process while maintaining hazard-free and race-free operations. This approach contrasts with one-step designs (Deeg et al. 2020), where complex algorithms are employed to construct the automaton without clocking. The programming in the FPGA occurs at the lowest level of abstraction to ensure that the structure is built in the same way, without the software attempting to optimize the structure. This is because the synchronous optimization process is used to build the structure. The asynchronous design cannot be simulated, so it must be built in accordance with the structure and verified with tests. This is to ensure that any known error models are excluded. The structural comparison of domino logic on the FPGA was conducted in (Deeg and Sattler 2024). This section will subsequently discuss the individual realizations in the FPGA at the low level.

Globally Asynchronous Locally Synchronous (GALS)

GALS is a design methodology for electronic circuits. It addresses the challenge of ensuring safe and reliable data transfer between independent clock domains within a system. A GALS system breaks down the circuit into independent blocks, each with its own local clock. These blocks communicate with each other asynchronously using handshaking protocols (Krstic et al. 2007). This allows for flexibility because blocks can operate at different speeds based on their needs, and scalability because the system can be easily expanded without worrying about the global clock. Furthermore, the GALS methodology results in reduced power consumption, as only active blocks are clocked, thereby increasing the system's power efficiency.

Asynchronous Handshake Protocol:

An asynchronous handshake protocol represents a communication agreement between two or more entities that allows them to exchange data without the necessity of a common clock (Chapiro 1984). In contrast to synchronous protocols, which rely on the timing of a common clock to regulate communication,

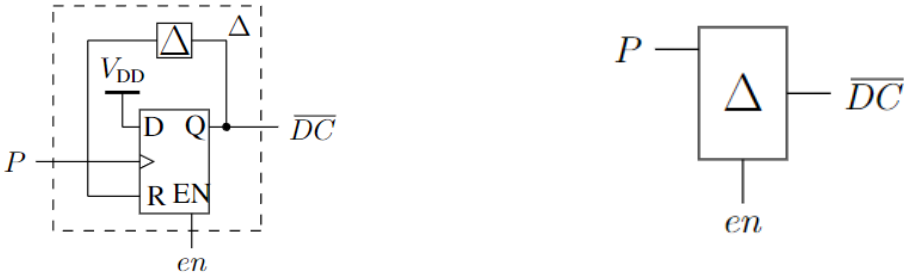
asynchronous handshake protocols employ a pair of signals to regulate data transmission. The initial signal is used to initiate the transmission of data (REQ), while the subsequent signal is utilized to confirm the successful completion of the data transmission (ACK).

Pulse Circuit

The purpose of self-locking is to enable the system to be unlocked again only once the circuit branches have been run through once and brought into a valid state. The input pulse circuit, which locks the input, can be seen in Figure 1.

Figure 1. *Pulse Circuit for Self-locking and Duty Cycle*

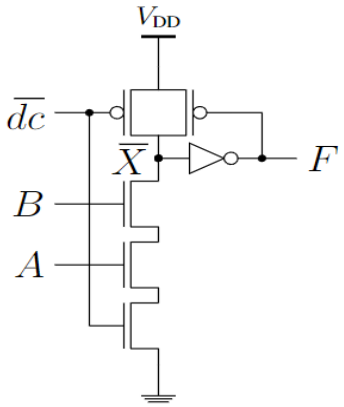
(a) Self-resetting D-FF **(b) Symbol**



The self-resetting input pulse circuit is employed for self-locking, whereby the input is directly locked following an initial pulse (REQ), and a precharge phase for the domino logic is initiated by the circuit's self- resetting feedback, subsequently disabling the input. The duration of the self-reset determines the length of the precharge phase. It is therefore necessary to ensure that the precharge phase is long enough for all internal nodes to be pulled to V_{DD}. Once this has been achieved, the dual-rail domino logic gates (DRDL) have no disjunctive outputs and then trigger the evaluation phase after the system has self-reset. The rising edge of dc then initiates the transfer of states and input signals to a D-FF at the input, where they are stabilized until the next evaluation phase. The circuit thus blocks the input, generates a duty cycle, and ensures stable signals during the evaluation step. Once the following block is done it will set an enable signal to 1 (ACK) and unlock the input again.

Domino Logic

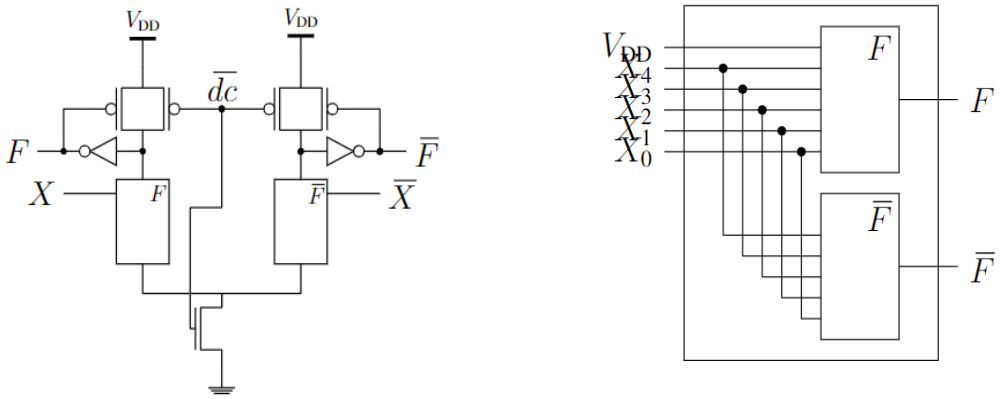
Figure 2. *Single Rail Domino Logic on Transistor Level (TL)*



The domino logic is an asynchronous logic family based on the principle of the domino effect (Hodges et al. 2004). The domino effect describes the chain reaction that occurs when one domino falls and knocks over the next in a row. In domino logic, these effects are used to transmit data through a switching network. Domino logic offers the aforementioned advantages of asynchronous circuits over traditional synchronous logic families. The general mode of operation of a domino logic gate can be divided into two phases: precharge and evaluate. A domino gate represents the fundamental unit of construction in domino logic. It is composed of two transistor circuits, one for the pull-up phase and one for the pull-down phase, which is composed into a single unit, see Figure 2, where an example for an AND2 domino gate is given. In the precharge phase, the inner node is charged to V_{DD}, and the logic state after the inverter is 0. If we then switch to the evaluate phase, i.e. our duty cycle switches from 0 to 1, the node is pulled to GND when the Pull-Down is active (i.e., the equation is fulfilled) and logic 1 is present at the output. Domino logic gates can now be connected in series and propagate through the pipeline. As the goal is to design asynchronously and recognize the transition through the gate, DRDL gates are employed, see Figure 3. These have an output F and the complementary output $\overline{F}$. The same principle applies here: first comes the precharge phase and then the evaluation phase. In the PC phase, both inner nodes are pulled to V_{DD}, the outputs are equivalent in their output value of logical 0, and then in the evaluation phase, one output becomes 1, while the other remains 0 due to the disjointness. This allows for the direct recognition of whether the domino gate has finished switching or not by linking both complementary outputs with an XOR. The dual-rail circuit thus provides a means of determining whether the circuit is in a valid state (i.e., the switched state) or an invalid state (i.e., the switching process is still underway). This information is always available, allowing the user to ascertain whether the circuit is currently occupied or ready for new data.

Figure 3. *Dual Rail Domino Logic*

(a) DRDL on TL **(b) DRDL as LUT6_2 on FPGA**



Pipeline with Completion Detection

Domino gates can now be composed serially in such a way that a pipeline is created, which is operated sequentially, i.e. not pipelined. This is achieved by assigning a separate state for each transfer of a 1, i.e. each domino effect to the next stage. In principle, however, real pipelining can also be used with the corresponding holding elements between the stages. However, this would not be a viable approach for the processing of instructions and the multicycle processor in question. The serial composition is performed by setting up the dominoes from the first stage f_0 to the last stage f_{n-1} to form $f = f_{n-1}(f_{n-2}(\ldots(f_1(f_0))\ldots)) = f_0 \circ f_1 \circ \ldots f_{n-2} \circ f_{n-1}$. Firstly, all domino gates are subjected to a preliminary charge which is designed to energize the internal nodes to a voltage of V_{DD} and set the outputs to a value of 0. The evaluation phase then pulls each DRDL gate in a path to 0, thus producing a 1 at one output of F and F. The system is then complete as soon as all DRDL gates are complementary to each other, which in turn unlocks the input. The input pulse therefore serves as a request signal and the en signal as an acknowledgment, so this is the asynchronous handshaking protocol. In the pipeline circuit, it is generally sufficient to check only the last stage for disjunctivity, as the last stage can only switch as soon as the previous one has switched. However, we have conducted a comprehensive analysis of all stages for disjunctivity, i.e. we have applied an XOR operation to each stage and rounded the results to ensure that each individual gate has switched and thus enhance safety.

Low-Level Primitives Design

The realization of our circuits is accomplished through the use of the Arty A7 Artix-7 FPGA Development Board, which is provided by Digilent and contains an FPGA manufactured by Xilinx Inc. The FPGA is programmed with the Vivado Design Suite (VDS) at a low-level in order to precisely define how the structures

are generated within the FPGA (what you see is what you get). The primitive libraries from ARTIX-7 (UG953 2012) are employed for this purpose. Two commands have emerged as pivotal: firstly, the ability to incorporate combinatorial loops into the constraints, and secondly, the don't touch commands to prevent the VDS from modifying any settings. The design is currently still completed manually but will be automated in the future. The logical design is based on look-up tables (LUTs). These LUTs are typically multiplexers that switch exactly one path to the output, depending on the input assignment. They are constructed in the shelf from NMOS pass transistors or transmission gates (Chiasson and Betz 2013). These low-level primitives can now be initialized as shown in the code snippet below.

Listing 1. *Low-Level LUT6_2 for AND2 DRDL Gate*

```
1.      LUT6_2_inst : LUT6_2 generic map (
2.      INIT => X"800000007FFF0000") -port map (
3.      O6 => f_int, -- 6/5-LUT output (1-bit)
4.      O5 => fbar_int, -- 5-LUT output (1-bit)
5.      I0 => '1', -- LUT input (1-bit)
6.      I1 => '1', -- LUT input (1-bit)
7.      I2 => x_int(0), -- LUT input (1-bit)
8.      I3 => x_int(1), -- LUT input (1-bit)
9.      I4 => _dc, -- LUT input (1-bit)
10.     I5 => '1'-- LUT input (1-bit)
11.     );
```

To realize dual-rail domino logic circuits, it has been decided that the LUT6_2 will be employed, as this structure allows for two disjoint outputs when input 5 is clamped to V_{DD}. However, this does entail a tradeoff in that one input is no longer available for use, and the number of table entries is reduced from 26 to 25. For designs with a maximum of five inputs, however, this has no negative effects. The LUT is initialized with a hexadecimal number, in this case, the realized function is $F = I_4 \wedge I_3 \wedge I_2 \wedge I_1 \wedge I_0$ for positive Pin F and $\overline{F} = \overline{I_4} \vee \overline{I_3} \vee \overline{I_2} \vee \overline{I_1} \vee \overline{I_0}$ for the complementary $\overline{F}$. To generate the duty cycle for our self-locking input pulse circuit, a D-FlipFlop is used that is permanently connected with one at the input and briefly goes to one on the positive edge of P and resets itself asynchronously after a duration τ_Δ. The low-level primitive of an FDCE, which is a D-FlipFlop with Clock Enable and Asynchronous Clear, is employed for this purpose. A code snippet for our feedback pulse circuit is provided in reference to the FDCE.

Listing 2. *Low-Level Self-Resetting Pulse Circuit*

```
1.      INIT => '0') -- Initial value port map (
2.      Q => dc, -- Data output
3.      C=> P, -- Clock input
4.      CE => '1', -- Clock enable input
5.      CLR => dc, -- Asynchronous clear input
6.      D=> en -- Data input
7.      );
```

Parallelization of Domino Gates

As previously stated, switching can also occur in parallel, rather than in a cascaded manner. This is because the switching processes have a clear direction and a clear end, due to the disjunctivity of the components and the self-clocking enables hazard-free operation. This is because the circuit only unlocks as soon as all the switching parts are disjoint to each other. It is therefore also conceivable, for example, to design the arithmetic logic unit (ALU) in parallel as a dual-rail domino gate to maintain the minimum processing delay by communicating with the controller using the handshake protocol and switching the individual gates in parallel until they are all disjoint. In this instance, the individual domino gates are composed in parallel to form $f = f_0(x) + f_1(x) + ... + f_{n-2}(x) + f_{n-1}(x)$

Implementation for RISC-V Processor

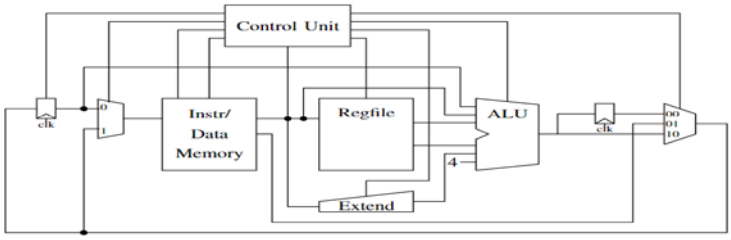
RISC-V represents a flexible and energy-efficient alternative to the dominant Reduced Instruction Set Computer (RISC) and Complex Instruction Set Computer (CISC) architectures. The simplified instruction set at the core of RISC-V is small and orthogonal, allowing for a thriving ecosystem of innovation. This simplified approach reduces the hardware requirements and improves overall performance by eliminating the complexity and overhead associated with complex instruction sets. The paper presents the design of a control unit for a 32-bit Turing-complete RISC-V architecture.

Synchronous Multicycle Central Processing Unit (CPU)

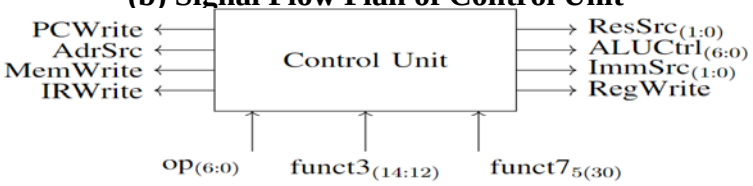
We will now briefly introduce the initial processor (Harris and Harris 2021), see Figure 4. It is a synchronous processor that is Turing complete, which means that it can calculate all Turing-computable functions. The processor is realized as a multicycle processor in order to design the different access times for different instructions in a way that allows for the division of an instruction into different individual steps. This is in contrast to a single-cycle processor, where the worst-case path for the entire instruction is considered. Instead, in this case, the worst case for the individual processing steps is considered. However, the processor employs a Harvard architecture, which is evident from the fact that it has separate data and instruction registers in a block random access memory (BRAM) (i.e., with two different addresses).

Figure 4. *Synchronous CPU and the Synchronous State Transfer Function*

(a) Architecture Synchronous CPU



(b) Signal Flow Plan of Control Unit



Synchronous Control Unit

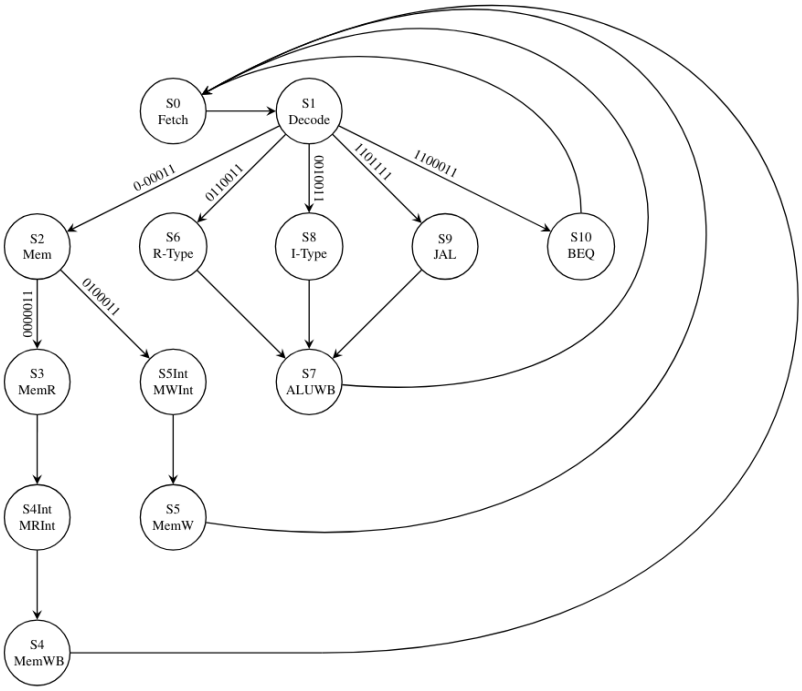
To be Turing-complete, the instructions given with the opcode in Table 1 are implemented. In order to process the instructions, an automaton is generated that was derived from RISC-V and uses the input opcode 6:3 to decode the individual states. In contrast to Harris and Harris (2021), a few states were added because the memory access requires two clock cycles, for example. Consequently, the multicycle processor is divided into the branches load, store, r-type, i-type, b-type, and jal, with the clock cycles split up in order to achieve shorter access times, see Figure 5.

Table 1. *Instructions*

Branch	OPCode	Name
L	0000011	Load
I	0010011	I-Type
S	0100011	Store
R	0110011	R-Type
B	1100011	B-Type
J	1101111	JAL

This results in the longest instruction load and the shortest branch-if-equal (BEQ). A single-cycle processor would now cover the worst case for all instructions, whereas the multicycle processor saves three cycles for NEQ. It is evident that the differing access times of the instructions justify the necessity of the multicycle processor. The automaton was then constructed as a Moore machine, with each state having a single output. The synchronous automaton was then designed at the high-level with optimizations from VDS.

Figure 5. *Automaton Graph of synchronous Moore Machine*



Design of the Asynchronous Controller

The circuit is then implemented in the synchronous RISC-V processor. The asynchronous handshaking protocol can significantly enhance the processor's performance, as it allows for different access times for different process steps (e.g., writing memory is much slower than addressing the reg file). Since the domino logic is realized as a pipeline, there is also a direct transfer to pipelines, but this application is not addressed further in this paper. In order to facilitate the design of a pipeline cascade, which is a more complex process in domino logic, we will implement a Mealy automaton that can generate different output values for its states depending on the input signal. In contrast to the synchronous Moore automaton, which has predefined processing times for the various instructions, the Mealy automaton is clocked externally by REQ and ACK. This means that the same states for different instructions can have different access times. Consequently, the states are superimposed and the edges are retained. Furthermore, self-locking can be applied to the output function, which negates the need for hazards and other potential issues. This results in a reduction in hardware requirements compared to the Moore Machine. The individual states were then encoded one-hot to enhance clarity in the domino output in the z-variables. The automaton graph for the pipeline can be seen in Figure 6 and its structure in Figure 7. Edge *A* is the opcode of the BEQ branch, since it only needs three states, *B* is given by R-type, I-type and JAL branches, *C* is the edge for the Store instruction, and the Load instruction gets to the last state [100000].

Figure 6. *Automaton Graph Pipeline*

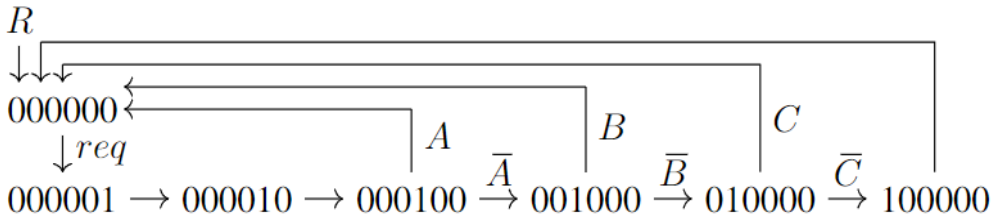
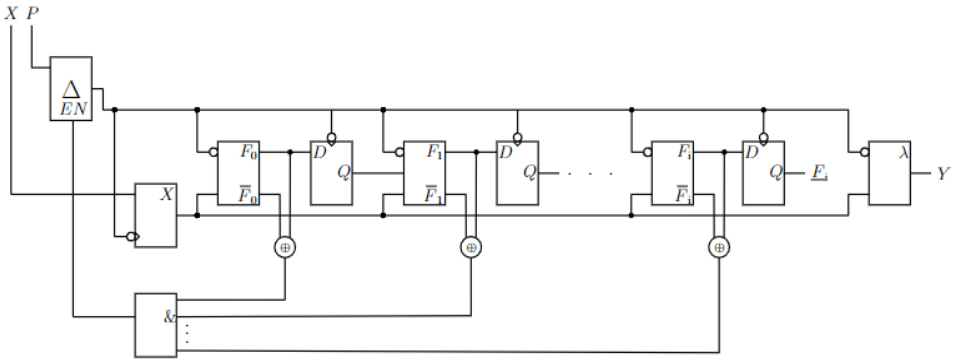


Figure 7. *Structure of realized Pipeline in FPGA*



Design of an Asynchronous ALU

To more effectively illustrate the advantages of the asynchronous handshake protocol, we have elected to configure the ALU as a parallelized, self-locking domino logic. Given the considerable time required to access the ALU, the self-clocked variant represents a promising improvement. In the following section, we will utilize the AND instruction as a case study in domino logic, with the objective of elucidating the design process. The starting point is an asynchronous ALU, which we wish to convert into a domino logic. The bitwise AND can be implemented straightforwardly by utilizing the AND structure of a domino gate and combining each position of the 32-bit word in dual-rail. This can be accomplished entirely in parallel. The independence of all dual-rail gates then indicates whether the ALU has undergone rounding, allowing the input to be unlocked by setting the en signal (ACK) to 1. The code snippet for the ALU's AND function as DRDL AND2 is listed below.

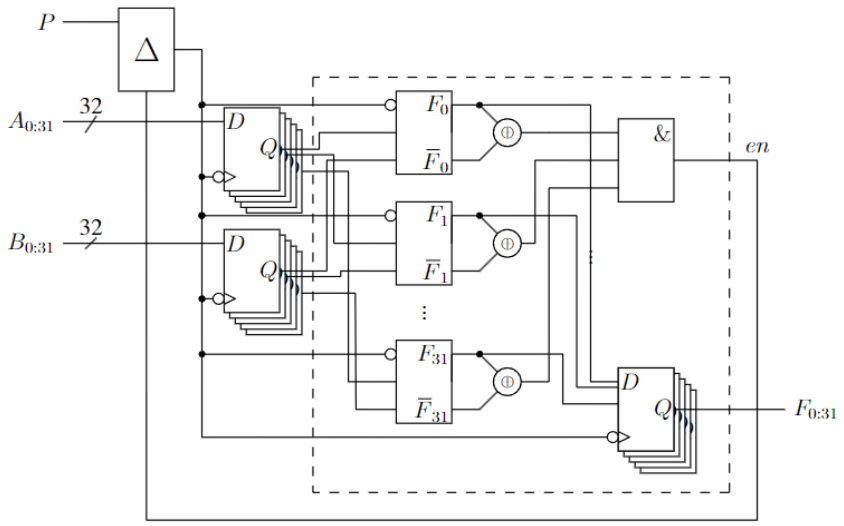
Listing 3. *Low-Level 32-Bit DRDL AND*

```
1.     MY_GEN : for i in 0 to 31 generate
2.     DominoGate: dualRail port
3.     map( dcbar => dc, x(0)=>'1',
4.      x(1)=>'1', x(2)=>reg_b(i),
5.     x(3)=>reg_a(i), f_out=>f_int(i),
6.     fbar_out=>fbar_int(i) );
7.     CompletionDetection:  xor_LUT port
8.     map( A => f_int(i),
9.     B => fbar_int(i),
```

```
    Y => xor(i)
    );
    process(dc)
    begin
    if(falling_edge(dc)) then
    f_out(i)<= f_int(i);
    fbar_out(i)<= fbar_int(i);
    end if;
    end process;
    end generate;
    process(xor)
    begin
    if(xor=x"FFFFFFFF")
    then
    en_int<='1';
    else
    en_int<='0';
    end if;
    end process;
```

The resulting structure of the AND for ALU in Self-Locking Domino Logic can be seen in Figure 8. Furthermore, the input incorporates a self-locking pulse circuit that generates a duty cycle, thereby initiating the precharge phase. This is followed by a scan of the source registers of the ALU multiplexers, after which the input is unlocked when each of the 32 DRDL gates has disjoint outputs.

Figure 8. *Domino Logic ALU*



Integration in the CPU

The self-locking machine can now be readily incorporated into the existing CPU and controlled via the clock, for instance. While this does not immediately enhance performance if the other processor components do not exhibit GALS

behavior, it demonstrates the simplicity of integrating self-timed circuits. Furthermore, self-timing necessitates fewer FFs, which consequently results in reduced power consumption. To illustrate the advantages of asynchronous handshaking, the DRDL ALU was also integrated. The controller oversees the operation of other components in a synchronous manner, while simultaneously initiating the asynchronous handshaking process with the ALU, thereby accelerating the execution of instructions that utilize the ALU.

Power Performance and Area (PPA) Results

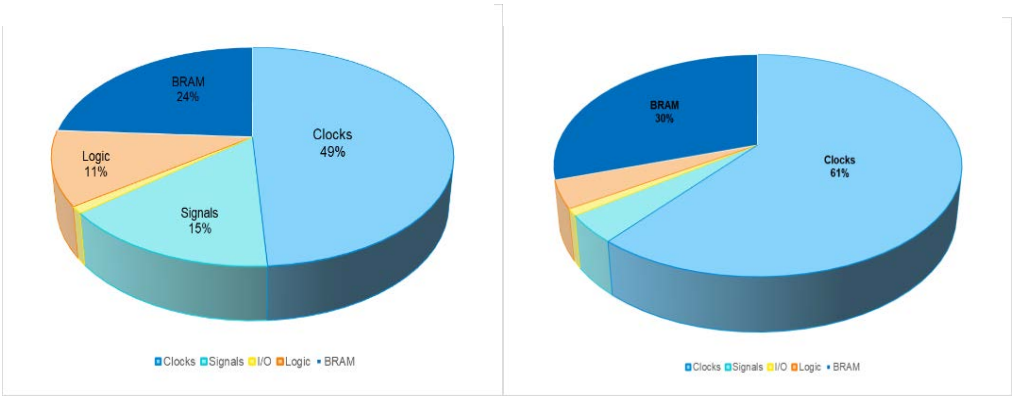
The PPA analysis of the implemented asynchronous processor on an FPGA definitively shows its efficiency and viability for various applications. This section presents the findings from the synthesis, implementation, and simulation processes using the Vivado Design Suite. The results are presented in three subsections: Power Analysis, Performance Analysis, and Area Analysis.

Power Consumption

The power consumption shares of the individual processors were obtained from the Vivado Power Analysis Tool, see Figure 9.

Figure 9. *Power Consumption of the CPUs*

(a) Asynchronous CPU **(b) Synchronous CPU**



The total dynamic power consumption of both the asynchronous and synchronous processors is nearly similar, which can be attributed to the parallel operation of the asynchronous processor. However, the asynchronous design achieves substantial power savings in the clock network, as evidenced by the lower percentage of power consumption dedicated to clocks in the asynchronous processor compared to the synchronous one. This highlights the efficiency of the asynchronous processor in minimizing clock-related power, which is a critical factor in overall power management and energy efficiency.

Performance Analysis

In this section, we assess the efficacy of our asynchronous CPU design by contrasting it with a synchronous CPU using the SPECint2000 benchmark suite. SPECint2000 is a well-established benchmark that measures the performance of CPUs with integer-heavy workloads, providing a comprehensive assessment through a variety of real-world applications. The benchmark is composed of approximately 25% loads, 10% stores, 11% branches, 2% jumps, and 52% R- or I-type ALU instructions. The diverse range of operations included in the SPECint2000 benchmark makes it an optimal tool for evaluating and comparing the performance characteristics of different CPU architectures. The objective of this analysis is to highlight the advantages and potential trade-offs of the asynchronous CPU design in comparison to its synchronous counterpart. A loop was constructed around the test code with a branch-if-equal (BEQ) instruction using a clock frequency of 100MHz, and the throughput of the asynchronous and synchronous CPUs, as well as the average duration per instruction were determined (see Table 2).

Table 2. *Performance Metrics*

Parameter	**Asynchronous CPU**	**Synchronous CPU**
Throughput (MIPS)	25.64	22.73
Average Latency/Instruction	39.5 ns	44 ns

The analysis shows, that the CPUs Performance for the SPECint2000 benchmark increased by around 10% simply by letting the control unit and the ALU do handshaking using DRDL Gates.

Area Analysis

The area analysis focuses on the utilization of FPGA resources, including LUTs, Slice Registers, F7 Multiplexers (F7 Muxes), and Slices. The asynchronous design utilized 6.67% of the available LUTs, indicating a moderate complexity in logic implementation. The design also employed 4.85% of the available slice registers, and leveraged 4.63% Slices. As anticipated, the area utilized exhibited an increase, yet remained within the anticipated range due to the implementation of DRDL gates within a single LUT.

Table 3. *FPGA Resource Utilization*

Resource Type	**Utilization in (%) Async**	**Utilization in (%) Sync**
LUTs	6.67%	6.32%
Slice Registers	4.85%	4.9%
Slices	9.27%	8.9%

Discussion

The PPA results indicate that the asynchronous processor demonstrates significant potential in terms of performance, which is crucial for performance-

critical applications. While there was a narrow change in power consumption, the area analysis shows a balanced utilization of FPGA resources, thereby highlighting the feasibility of implementing such designs within reasonable silicon area constraints.

Conclusion and Future Work

This work proposes an asynchronous RISC-V CPU design based on self-locking domino control. The asynchronous approach offers advantages over traditional synchronous designs in terms of performance, power consumption, and modularity. The paper describes in detail the design and implementation of the asynchronous control unit using domino control on an FPGA development board. The control unit is designed for a Turing-complete 32-bit RISC-V architecture. A significant aspect of the design is the self-locking mechanism, which ensures that the circuit is not released until all processing stages have been completed. This eliminates the need for a global clock and simplifies error-free operation. Furthermore, the paper discusses the possibility of parallelizing the ALU using domino control to further improve performance. Subsequently, the paper illustrates the straightforward integration of the asynchronous control unit into an existing synchronous central processing unit (CPU), thereby demonstrating the potential benefits of self-timed circuits. Ultimately, the PPA analysis of the implemented asynchronous processor on an FPGA substantiates its considerable potential for diverse applications. The power analysis indicates that while the total dynamic power consumption of the asynchronous processor is comparable to that of the synchronous processor, it achieves a significant reduction in power consumption within the clock network. This underscores the asynchronous processor's efficacy in curbing clock-related power consumption, a pivotal aspect of comprehensive power management and energy efficiency. A performance analysis conducted using the SPECint2000 benchmark suite revealed that the asynchronous processor exhibited superior performance compared to the synchronous processor, demonstrating a 10% increase in throughput and a reduction in average latency per instruction. This performance enhancement is achieved through the use of handshaking with DRDL gates in the control unit and ALU. The area analysis indicates that the asynchronous design employs FPGA resources in a moderate manner, exhibiting a slight increase in LUT, slice register, and slice utilization in comparison to the synchronous design. Despite this increase, the resource utilization remains within acceptable limits, thereby substantiating the feasibility of implementing the asynchronous processor within reasonable silicon area constraints. In conclusion, the asynchronous processor exhibits notable advantages in terms of power efficiency, performance, and area utilization, thereby establishing its viability as a potential solution for performance-critical applications.

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Transforming CS Curricula into EU-standardized Micro-Credentials – The Hard Parts

By Till Hänisch[*], Lea Schmitt[±] & Franziska Schütz[°]

Since the working environment continues to develop, mobility and flexibility are becoming increasingly important for both companies and employees. Therefore, universities need to transform their study programs into smaller units, so called micro-credentials, which offer flexible and individual learning pathways. To permit EU-wide exchange, micro-credentials have to be recognized and quality-assured and the certificates have to provide a transparent and universal skill set. The process for converting modules into micro-credentials still contains some open issues: micro-credentials typically have a size between 1 and 3 ECTS which means that bigger modules must be broken down into smaller parts. The division of units leads to the problem of assigning especially transversal skills and how to assess, verify and certify them. Additionally, it is not yet clear how micro-credentials are to be classified in the European Qualification Framework (EQF) as modules are accredited in study programs within a certain EQF level. Since micro-credentials can be taken stand-alone this is not always possible. This paper discusses these problems and gives an overview of the state of the art for solving some of them. Therefore, the concept of partial skills is introduced.

Keywords: *micro-credentials, lifelong learning, skills, partial skills*

Introduction

Micro-credentials are the EU-way of establishing flexible learning pathways in Europe. Micro-credentials (MCs), "the record of the learning outcomes that a learner has acquired following a small volume of learning" (Council of the European Union 2022, p. 5), are meant to allow the description, certification, and recognition of skills in a transparent and portable way across universities, especially in different countries. One target of MCs is to enable members of the workforce to adapt quickly to changes in the labour market and gather required future skills. They allow the recognition not only of skills acquired during a study program but also of practical experience and lifelong learning activities. Therefore, a second target is integrating flexible learning pathways into the classic forms of education defined in the European Qualification Framework.

Universities can convert existing programs to MCs by unbundling them: Existing modules are broken down into smaller units of typically 1-6 ECTS which are described and offered as MCs. A core feature of MCs is that they can be stacked

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to larger units. At least in theory, complete programs can be converted to stacks of MCs by rebundling.

To use the full potential of MCs, it is necessary to convert all elements of existing modules like skills, outcomes, assessment, prerequisites, qualification level, size etc. to a standard EU-wide recognizable form.

In our previous paper (Berkling et al. 2023) we described this process and the lessons learned during converting modules from an existing Computer Science Curriculum at DHBW to MCs. In this paper we will focus on one aspect of the bundling/unbundling part: how to handle (assess, document, certify etc.) skills at the level of an individual MC, which are developed and assessed over the course of a whole module resp. a stack of MCs.

Problems with Micro-credentials

Implementing micro-credentials (MCs) has several known problems, starting with the name. There are still some global ambiguities and different understandings regarding the nomenclature of MCs. Many synonyms are used in the literature for what the European Union calls MCs, such as digital badges, open badges or mini degrees (European Commission et al. 2020c, p. 38). Moreover, there are various educational institutions that offer small programs with certificates under different names, such as “NanoDegrees” or “MicroMasters”. Since there is no common and standardized definition for MCs, this impedes the validation and recognition outside of the respective provider (European Commission et al. 2020a, p. 10). The lack of a commonly defined standard and quality assurance can easily lead to uncertainty and doubts about the quality of MCs (McGreal et al. 2022, p. 293). A coherent and consistent approach to MCs is necessary to solve all those barriers successfully (European Commission et al. 2020c, p. 42). Therefore, the agreement about a common and generally recognized definition and implementation of MCs within an alliance must always be the first elementary step.

Furthermore, it needs to be clarified if and how MCs can be classified within the European Qualification Framework (EQF). Currently, the EQF doesn’t have a clear mapping or level assignment for MCs. MCs are often generated out of study programs in higher education. These programs are accredited within a certain EQF level which are the levels 6 and 7 for undergraduate and postgraduate studies. However, since the European Union intents to use MCs as an approach for lifelong learning, they can be taken stand-alone and completely independent from a study program (Council of the European Union 2022, p. 5). A single MC is not necessarily classified in the EQF level of the whole study program. Maybe the European e-Competence Framework (e-CF) offers an idea: the e-CF provides a common language for skills and competences in the ICT workplace by identifying competences in five proficiency levels e-1 to e-5 which can be mapped to the EQF levels 3 to 8 (European Committee for Standardization 2014, pp. 17, 42). Each competence within the e-CF is mapped to a corresponding e-CF level and can therefore be mapped to a certain EQF level (European Committee for Standardization 2014, p. 10). However, this is not standardized and specialized

only for the ICT sector, so the question of classification MCs within the EQF remains unsolved.

Besides that, the recommended size of MCs is globally widely discussed. According to a survey that was undertaken by the Consultation Group on micro-credentials of the European Union (European Commission et al. 2020b) the recommended number of ECTS for MCs varies. The group suggests that "3 and 5 ECTS seem to be ideal sizes for micro-credentials" (European Commission et al. 2020b, p. 19), although some respondents of the survey confer a minimum of 5 ECTS per MC (European Commission et al. 2020b, p. 9). The New Zealand Qualification Authority defines an upper and lower limit between 5 and 40 ECTS in size (European Commission et al. 2020b, p. 11), but there are many others like 2-6 ECTS for single MCs.

These formal problems are at least partially solvable by formal means, for example by making information like EQF level optional in the description of MCs. There are harder problems, especially the definition of earned skills and outcomes.

Of course, there are several initiatives like ESCO[1] for standardizing skills on different levels but as ESCO refers to the skills requested on the European labour market it does not always entirely fit to the learning outcomes defined in higher education. Currently, there is (as far as known to the authors) no universally accepted skill framework which is widely used and leads to a broadly understandable skill set (there are some more detailed points about that in the section: Existing Approaches). This impedes the process of defining standardized skill sets in MCs which is still an unsolved problem. However, much harder is the question, how to quantify skills and/or put them in a hierarchy to group related things together across different domains which will be discussed in detail in the next sections.

Currently, most universities do not follow common standards when describing competences and skills in module descriptions. "Traditionally higher education was relatively explicit about the knowledge (outcomes) to be achieved, or at least the knowledge covered by the curriculum. It was however somewhat less explicit on the skills or competences required for the award of a given qualification. Competences, such as those of critical evaluation, were and are embedded or implicit in the assessment values and practices." (Bologna Working Group 2005, p. 63). The same goes for ethics, security, or sustainability and other transversal skills. These future skills are hard to get from one single module or MC but will be the result of a longer process acquiring them from several distinct activities in most cases. Therefore, these skills are often defined on the level of study programs, not individual modules. But how can we express that, when the students take (only, maybe in the far, bright future?) individual MCs?

But let's start with the simpler case of unbundling a module into several MCs, which are then rebundled into a MC stack. In our previous paper (Berkling et al. 2023) we used an introductory course on Software Engineering as an example. Out of this module we created three MCs (Specification, Design, Implementation) which can then be rebundled as a MC stack. There are skills like "organising,

[1]https://esco.ec.europa.eu.

planning and scheduling work and activities" which clearly belong to one of the MCs inside the stack, in this case to the third (Implementation). But transversal skills like "using digital tools for collaboration, content creation and problem solving" are harder to attach to a single MC. Clearly, they are taught (and assessed) in the original module and taking part in the whole stack which will deliver the same outcome. But to which MC should they be assigned? Probably (in some kind) to all of them. But what quantity (or even quality, see Section: Existing Approaches) of this skill is gathered in each of the three MCs?

If one student (for example because he is not in the CS-program but in Health) completes only the first MC of the stack, another one all parts (see Figure 2 for an example), how can we identify the difference in skills acquired? Obviously, they should not have the same set of skills. If transversal skills are distributed over the MCs in the stack, it is necessary to define and certify all the skills of the original module to a learner. The interesting question is, if these (probably transversal) skills should be indicated at more than one MC. If not, then two students, one taking the course as a module will have more skills than the one, who takes it as a MC stack. The skills could be weighted in some way, for example proportional to the size of the course (see Skills Hours n Uk QAA Project Section), but this brings its own problems, especially with interoperability (see Discussion Section).

There is (as far as known to the authors) no standard way of handling this problem. Of course, different approaches would be possible: we could assign points or badges or some other semi-quantitative attributes to a skill for each MC. But that would be hard to get consistent across platforms/universities. Maybe that only makes sense in one ecosystem to express things like: "To get the skill 'using digital tools for collaboration, content creation and problem solving' you need to take all three parts together or maybe take only one of these but then you need other MCs which provide the missing amount of that skill."

So, we have to differentiate between the internal documentation of skills a student has and the external view. In the next chapters we will describe a way, which is simple enough to be understandable for external users but allows students to collect skills over the course of a number of MCs and get them certified as the outcome of a MC stack.

The following approaches of other universities solve part of that problem, but the question of consistency across universities or countries are basically unsolved.

Existing Approaches

The educational system of Ontario is currently presented with a similar problem: within the educational system, in particular the higher educational system, barriers towards the stackability of micro-credentials (MCs) have been identified. The major obstacle is the lack of standardized, comparable, transparent, and verified information about obtained competences and skills from accomplished MCs (Usher et al. 2023, p. III). Ontario's Higher Education Strategy Associates detected increasing inquiries concerning the stacking of MCs into diplomas and degrees,

particularly stacking obtained MCs from several (two or even more) different institutions and educational providers.

Due to a lack of transparency concerning relevant data on e.g., prerequisites, learning outcomes, etc., certifying educational institutions are presented with difficulties comparing MCs to formal courses in order to assess equivalences. (Usher et al. 2023, p. III).

According to the European Commission's definition of MCs, stackability and portability of accomplished credentials are key characteristics of MCs. Therefore, transparency of key data of MCs is crucial to provide possibilities to build on prior certified learning experiences with incremental credentials to foster higher proficiency levels in respective learning areas and topics (Usher et al. 2023, p. 5). Detailed information on obtained competences and skills could reduce replication and foster inter-institutional recognition (of MCs) (Usher et al. 2023, p. 4).

With regard to portability and appraising obtained skills and competences, defining and designing interrelated MC stacks within one institution would usually be preferable. In particular, information about included and imported transversal skills within MCs is primarily available in the respective offering institution. Finding and researching for detailed information of learning-outcomes in MCs offered by other institutions would require a great amount of personal resources and time exposure at institutions given the fact of very limited credit value in order to integrate a single extra-institutional MC into a module or stack (Usher et al. 2023, p. 26). Their conclusion is that MC stacks should be preferably designed and defined within just one institution.

Obviously, this would eliminate most of the problems mentioned above. But it would unnecessarily limit the usability of MCs, especially for cross-domain and cross-university usage. This would limit the use of MC stacks to mostly internal use cases. So better ways should be defined. The only real solution to this problem would be to define and use standardized skill descriptors and quantifications (see LCAMP Knowledge Graph Section).

Skills Hours in UK QAA Project

In October 2022 the Quality Assurance Agency for Higher Education (QAA) published the project report "Collaborative Enhancement Project Report on badging and micro-credentialing within UK higher education through the use of skills profiles" (Ward et al. 2023, p. 2). This report included case studies from six UK universities concerning skills profiling approaches to granularize university courses and modules. The project pursued the objective to present solutions to reduce assessment workloads albeit increasing development of granular degree courses and opening recognition and accreditation pathways of LinkedIn Learning credits (Ward et al. 2023, p. 3).

The QAA project pursues the approach of translating learning outcomes into skills hours to develop skills profiles. The project uses six skills themes and 25 skills categories as a basis to define skills profiles within curricula. These six themes are classified alphabetically from A to F and imply understanding, context,

solution, delivery and behaviour. The secondary skills categories refer either to subject-based or transferable skills and invoke one skills theme. In the curricula of university courses or modules each learning-outcome can be translated into or matched to the most appropriate one or several skills of the list of 25 subject specific and transferable skills categories. In order to obtain specific skill hours within a curriculum, the skills categories hours are calculated pro-rata from learning hours including assessment learning hours, its weighting, and referring learning outcomes hours (Ward et al. 2023, p. 5).

The contributing UK universities instance an example of a university module with 200 learning hours and two assessments with weighting 60:40. According to that example one assessment would require 120 learning assessment hours, the other one would require 80 learning assessment hours (Ward et al. 2023, p. 5). As subject specific skills categories can be matched quite distinctly to the learning outcomes of said university module and respective assessment, subsequently the required learning hours for each learning outcome and skills category can be estimated. As a result, the expenditure of each subject-based skills category can be calculated and displayed transparently.

Regarding the transferable skills categories, the estimated skills hours are calculated in a similar approach. However, transferable skills present a characteristic to apply to multiple learning outcomes. In the case study, the University of Bath pointed out this challenge while translating learning outcomes into skills. Therefore, the individual total hours of a transferable skills category need to be calculated as a function of the multitude of skills required for the learning outcome and thus a percentage of the respective learning outcome hours and summed up in a second step (Ward et al. 2023, p. 6). The researchers found that multiple skills could be identified for one learning outcome in a curriculum and therefore needed to split the skills hours among the associated transferable and subject-based skills (Ward et al. 2023, p. 24).

The approach provides specific information on required hours to obtain specific skills. Thereupon this approach by six UK universities of the QAA project could also be used to make apparent the extent to which the respective skills were imparted in the respective micro-credential as part of a stack with exactly calculated skills hours. This could clearly show if transversal and soft skills in particular have only been partially applied in a course due to granularization of university modules and greater courses.

For better illustration, the following skills hours approach is applied to the MC Specification from the MC stack Software Engineering with one assessment lasting 120 minutes.

First, the learning outcomes must be mapped to the skills categories of the QAA project, see Table 1.

Table 1. *Mapping from Learning Outcomes to Skills Categories of the QAA Project*

Learning Outcome	Skills category (QAA Project)
They know the methods of the respective project phases and can apply them. They can use tools for collaboration and problem-solving.	S4D - Subject Based Process & Production: Actions or steps taken to achieve a particular result
The students can competitively evaluate solution proposals for a given problem and justify their designs and solutions. They can competitively assess, select, and critically reflect upon solution proposals for a given problem.	T14E - Transferable Evaluation: Asssessing the amount, number or value of something
The students can engage with domain experts in discussions about problem analyses and solution proposals, as well as about the interconnections of individual phases. During the discussion, they can critically engage with various perspectives. They can orally and in writing present their designs and solutions. They can handle conflicts and resolve them constructively.	T19F - Transferable Communication: Conveying meaning to others
They can build and further develop teams. They can handle conflicts and resolve them constructively. They can pass on and support skills. They can provide each other with constructive feedback. They can effectively collaborate within a team in complex projects.	T18E - Transferable Collaboration: Processes where two or more people work together to complete tasks or goal

After mapping the learning outcomes of the MC curriculum to the skills categories of QAA, the calculation of skills hours referring to the respective described learning outcomes can be applied, as shown hereafter.

Table 2 shows the calculation for the subject-based skills categories which leads quite easy to the subject-based skills hours.

Table 2. *Mapping and Calculation of Subject-based Skills Hours*

Assess-ment	Assessment Learning Hours	Learning Outcomes	Learning Outcomes Hours	Subject-based skills categories	List of subject-based skills categories	Subject-based skills hours
1	120	1	30	S1A	S1A	30
		2	30	S4D	S4D	60
		3	30	S5E	S5E	30
		4	30	S4D		

The calculation of the transferable skills hours needs to follow the amount of learning outcomes for each skills category, so the calculation is more complicated (see Table 3 and Table 4).

Table 3. *Mapping Learning Outcomes to Transferable Skills Categories*

Assess-ment	Assessment Learning Hours	Learning Outcomes	Learning Outcomes Hours	Transferable skills categories
1	120	1	24	T14E, T7C, T15E
		2	24	T14E, T7C, T15E, T9D
		3	24	T19F, T8D
		4	24	T19F, T5B, T17E
		5	24	T18E, T19F

Table 4. *Calculation of Skills Hours for Transferable Skills Categories*

List of Transferable skills categories	Calculation	Transferable skills hours
T14E	24 x ⅓ + 24x ¼	14
T7C	24 x ⅓ + 24x ¼	14
T15E	24 x ⅓ + 24x ¼	14
T9D	24x ¼	6
T19F	24x ½ + 24x ⅓ + 24x ½	32
T8D	24x ½	12
T5B	24x ⅓	8
T17E	24x ⅓	8
T18E	24x ½	12

LCAMP Knowledge Graph

In the LCAMP research project, Learner Centric Advanced Manufacturing Platform, learning pathways for employees in advanced manufacturing are developed for effective re- and upskilling particularly in the advanced manufacturing sector. In this research project, the transition to higher levels of education as well as the reconciliation of academic and economic requirements of the labour market are important in the description of the MC for the development of learning skills, so that the greatest possible transparency is created for employers for the comparability of information in certificates and demanded skills in job profiles.

A three-axis knowledge graph is used as a basis for describing and classifying the existing competencies and skills of the learners presenting different educational backgrounds for better matching with regard to appropriate re- and upskilling pathways. In order to obtain the most accurate appraisal of available competencies from respective learners it is crucial to reflect on different influential factors for competencies. As a result, one axis of the matrix displays learners pertinent (work) experience of applying a certain competence or skill. Furthermore,

the matrix implies one axis referring to classification based on certifications and qualifications, such as the EQF level. The third axis of the LCAMP knowledge graph matrix depends on proficiency levels as a sectoral and occupational axis regarding thematic depths of competencies and skills.

While relevant pertinent work experience can be depicted relatively clearly on the graph scale, the two other axes of the LCAMP knowledge graph are more difficult to appraise, but decisive in the assessment of the respective skill or competency maturity. Regarding the occupation and sectoral axis, it is important to distinguish how deep the learner's expertise is for a particular one, however the proficiency level does not always increase with a higher educational degree. For example, employees working in the mechanical engineering industry generally are required to present skills referring to the use of simulation technologies. Regarding possible working fields for above mentioned degree alumni, requirements to apply this skill or competency might be drastically different depending on the industry sector. For example, in a specialized industry such as pharmacy, you have the handling of a specific software in addition to the general skill, which e.g. are not used and needed in the same job description in the automotive industry with different product and safety requirements.

Laboratory skills can be even more diverse, which can be very specific within industries. Laboratory knowledge in the field of materials testing, e.g. in the metals industry are fundamentally different from the skills required for laboratory activities in biotechnology. Not only are there sectoral differences, but also qualifying ones, as certain qualifications and certificates have to be shown in each case, so that the proficiency of the respective learners also increases. With higher qualifications, competence profiles can also change.

The representation of all three matrix dimensions is therefore particularly important for mapping the interaction on the respective competency and skill maturity in the transition from Dublin Descriptor level DD1 to Dublin Descriptor level DD2 as well as for the determination of the expression of skills in the professional and academic environment for comparison and adaption. To illustrate this, here is an example for a warehouse logistics specialist:

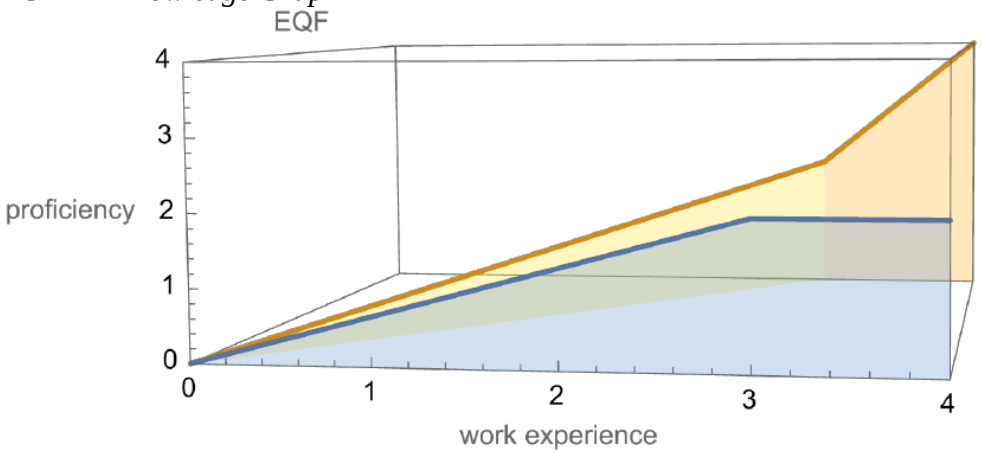
Starting with the work experience of an employee with this qualification, a learner is obliged to have a pertinent vocational education and training in a company for three years in order to obtain the qualification as a warehouse logistics specialist referring to EQF level 4. With this in mind, the appropriate figures on the temporal as well as on the classification axes can be declared. Regarding a specific competency required for this qualification e.g. supply chain management, several skills must be obtained by employees with said qualification including project management, problem solving, negotiation, time management, communication skills, adaptability, inventory management, logistics and analytical skills. The required project management and problem-solving skills are solely applied in the field of logistics, so there is a deep knowledge of applying and developing solutions and innovations to problems occurring in warehouses such as spatial capacity shortages or directives of lawful storage. The skills problem solving, project management and innovation management are also required in

several other occupations and are directly linked to respective sectors or environments due to laws, regulations, and products specialities.

Although, a warehouse logistics specialist does not present a high EQF level, the employee holding this qualification can demonstrate a higher proficiency level of a respective skill or competence due to working experience and sectoral specifications where skills are required to be applied to on a regular basis. In order to determine a more precise figure to that specific skill proficiency level, a fuzzy calculation needs to be done in consideration of all three matrix dimensions affecting the value that needs to be calculated.

As shown in Figure 1, the skill range can vary depending on the homogeneity of the working environment for warehouse logistics specialists with the same vocational education and training. The more varied the tasks and the associated skills required to perform them, the higher the proficiency level.

Figure 1. *Representation of Different Levels of a Warehouse Logistics in the LCAMP Knowledge Graph*

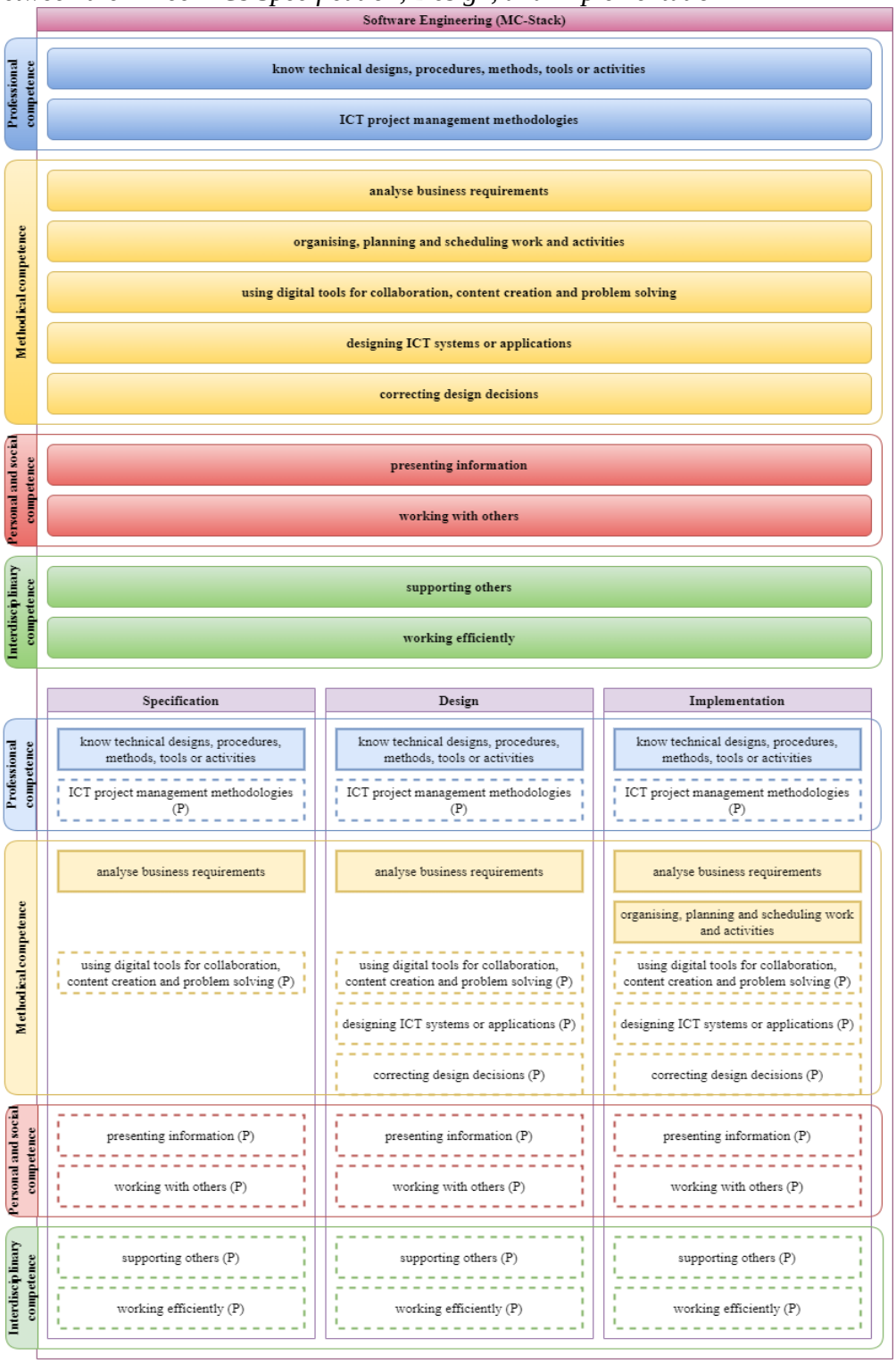


Partial Skills

The main contribution of this paper is to define the concept of partial skills as a way to express the fact that aspects of a skill are taught in a certain micro-credential (MC) while not covering the whole breadth or depth of it. Only the combination with other MCs makes it possible to acquire the skill and get it certified. This can be done in the form of a MC stack.

As an example, let's consider our example module "Software Engineering". It consists of three units (MCs), covering a typical software engineering process: Specification, Design, and Implementation. In each of those, the students will gather phase specific knowledge like for example "analyse requirements" in the first phase, "designing ICT systems or applications" in the second and "continuous integration" or "correcting design decisions" in the third. The specific knowledges are easy to assign to the individual small MC most of the time. That's because the decomposition of the topic into these units typically depends on knowledge (DD level 1 and 2) rather than skills.

Figure 2. *MC Stack Software Engineering with Some of the Obtained Skills by Completing the Whole Stack and Distribution of the Skills and Partial Skills between the Three MCs Specification, Design, and Implementation*



The problems start with the higher levels, like "presenting information" or "working with others" (DD level 3 and 4). And this gets even worse with skills like "working efficiently", "supporting others" or "thinking creatively and innovatively" (DD level 5). In these cases, the knowledges and skills are assigned to individual MCs, if they are covered only in this MC. If not, they are assigned as a "partial skill" with a special identifier (in this case "(P)") like "presenting information (P)". That means that they are not fully learned and/or explicitly assessed during this MC. Because of that, they are not shown on the external level on the MC certificate, but only defined on the internal level. The corresponding MC stack, in this case "Software Engineering" = {Specification, Design, Implementation} has all the original skills assigned to the module. Figure 2 shows the skills obtained by successfully completing the entire MC stack as well as the distribution of skills and partial skills in the individual MCs Specification, Design, and Implementation.

Typically, MC stacks are defined at the recognizing institution, so the information about the partial skills acquired through an individual MC is lost. To solve this, we propose the definition of a special kind of MC stack – skill-oriented MC – for this purpose. This stack is defined and assessed in full by the offeror of the MCs and can be recognized in full by any other institution. This process might need kind of a clearing house to finally decide if those future skills are given by a stack in the expected quality and quantity and defines, for what programs (at which EQF levels?) they can be recognized.

Discussion

For external institutions as well as employers it is difficult to understand what skills have been obtained within a micro-credential (MC) and to what extent those imparted skills have been applied and assessed. The source of this problem of comprehension can be drawn to the description and phrasing of learning outcomes in curricula which are often depicted in academical or very generic terms instead of skills terms used within the labour market.

Using standardized terms to describe learning outcomes of MCs could present one solution to foster mutual transparency and understanding among academia and the labour market. A jointly used skills framework with common nomenclature to describe learning outcomes in skills and competences is crucial for this approach. At the moment, there are various skills frameworks to be found and used to describe and categorize competencies with different terms (Ward et al. 2023, p. 63). In each of the frameworks similar terms for competences and skills can be detected, however, the different competences and skills frameworks also demonstrate specific terms and descriptions of skills which are particularly used in the referring industry sector. With regard to Industry 4.0, most used and known skills and competence frameworks encompass the models of SFIA 8, KETs Skills framework and "A Competency Model for 'Industrie 4.0' Employees" by Prifti. The Prifti model and SFIA 8 model are competence-based frameworks with a similar target group. Whereas SFIA8 was developed for the ICT community, using

terms well-known to business experts and technology experts (Seward 2021), the "Competency Framework" by Prifti focuses on competences required from employees with degrees referring to either computer science, engineering, or information systems (cf. Prifti et al. 2017, p. 10). The KETs Initiative study by PricewaterhouseCooper focused on demanded skills for key enabling technologies and the developed framework addresses employees working in the industry sector of advanced manufacturing and key technology users (European Commission et al. 2016, p. 36). Regarding the competence "negotiation" you can find the same term for this competence in the framework by Prifti, the KETs model uses the skill "deal negotiation skill" whereas in SFIA8 the competence cannot be found.

The lack of a commonly used framework impedes the process because the terms used in the varying frameworks differ drastically and so skill terms to describe learning outcomes cannot be compared accurately among providers and employers. Furthermore, to use the approach of the QAA and exactly and transferable depict the skills hours in MCs, a unified scale needs to be developed and presented, a scale to demonstrate with which number of skills hours a transversal skills category is considered to have been acquired and not only taught as a partial skill, so other HEIs and educational providers can estimate ones proficiency or skills acquirements. Moreover, that approach can also be beneficial for learners to understand their own development better and make more informed choices on further required skill developments (Ward et al. 2023, p. 68).

Conclusion

If there is no commonly accepted scale to quantify the amount of transfer of a skill in one micro-credential, a less precise method - partial skills - can be used. Primarily intended for internal use or in a small alliance, it is easy enough to be understandable for external users as an indicator, that a certain skill has been imparted at least partially, whatever that means.

Maybe finding a method to describe the achievement of a partial skill is a more general problem than just in the context of micro-credentials: it is a general problem, if transversal skills are not taught separately in special modules about for example critical thinking, but are distributed over more than one, maybe even many modules.

For example, at DHBW many transversal skills (like project management or critical thinking) in technical programs are taught separately in a module called "Schlüsselqualifikationen" (key qualifications in English). They are only mentioned as soft skills in some other technical project-oriented modules like "Software Engineering" where students work on a project and learn for example project management by doing it.

Our anecdotal experience shows that the students learn these skills better in the technical context of their discipline. So, it might make sense, to abandon the special modules for transversal skills and integrate them into technical courses. Recent EU-projects indicate this trend as well, for example "Transversal skills cannot be learned on their own. In fact, the opposite is true, since they are skills

that must be achieved in a social context with other people. For that reason, these skills are often taken for granted in the educational context in general, and there is evidence that more attention needs to be placed on these skills in the HE context specifically" (Carrió 2022). Similar results can be seen in other projects, for example (Cimatti 2016).

This change would mean that even when not using micro-credentials, a way to specify and collect partial skills in these areas is needed for the definition of transversal skills as outcomes of individual modules on the level of study programs.

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A Visual Cross-software Evaluation Platform for Perseveration and Revitalization of Historical Villages: Application in Qinchuan Historical Village, Zhejiang Province

By Junpeng Fan[*]

The preservation and revitalization of historical villages have emerged as prominent topics within the realm of Chinese cultural heritage preservation. However, persistent challenges arise from the lack of spatial digital information and the complexities involved in sampling and analyzing these historical sites. An emerging field of inquiry addresses the effective analysis of the spatial elements of historical villages for design evaluation and research in the context of their preservation and revitalization, with the objective of aligning them with contemporary needs. This research integrates Unmanned Aerial Vehicle (UAV) 3D oblique imagery and Computer Vision (CV) techniques to replace traditional data collection methods, thereby addressing challenges caused by insufficient data and providing a more economical and efficient solution. Furthermore, it establishes a linkage between Rhinoceros-Grasshopper (GH)-Unity 3D to create a novel cross-software evaluation platform. This platform assists designers in researching and analyzing the spatial aspects of historical villages and various streetview elements, including building, sky, ground, tree, door, window, water, plants, person, and transport, thereby facilitating the assessment of their impact on the preservation and revitalization of traditional historical village.

Keywords: *computer vision, parametric design, villages protection and renewal, oblique imagery, cross-software*

Introduction

The safeguarding and transmission of tangible and intangible aspects within traditional villages, the improvement of living conditions in these areas, and the maintenance of the spatial layout characteristic of traditional villages have become focal points in the field of traditional village preservation. Currently, conventional approaches for analyzing and appraising historical villages often rely on labor-intensive data collection processes, typically involving on-site investigations or photographic assessments. These methods are expensive and suffer from the loss of historical documents, lack of data information, and sampling difficulties due to geographical or topographical factors. Consequently, the current pivotal issue lies in exploring how to leverage and integrate advanced computer technology to promote the revitalization of historical villages more scientifically and efficiently, in contrast to traditional and less accurate analysis and evaluation methods.

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This research examines the potential of Computer Vision (CV) technology for driving automatic parameter analysis to generate street view facade designs through parameterization. The computer-aided design software employs 3D technology to develop visual design tools and introduces two key innovations. Firstly, it seeks to employ CV technology to segment and identify images or point clouds associated with existing building structures and environments. This method combines the strengths of CV technology with parametric design methods to identify 10 elements (building, sky, ground, tree, door, window, water, plants, person, and transport) in historical villages and traditional villages undergoing revival under heritage protection. Secondly, the research employs the game development software Unity to create a cross-software evaluation plug-in, with the aim of enhancing efficiency for professionals in the industry. The viability of this technology will be rigorously evaluated in Qinchuan, a representative traditional Chinese village.

Literature Review

Key Factors in Historical Village Preservation and Revitalization

The preservation and revitalization of historical villages require a comprehensive approach that considers various design scales. At the general plan scale, factors such as geographical environment, climate conditions, and hydrological conditions play a crucial role in the preservation and revitalization of historical villages. The geographical environment, including mountains, plains, or valleys, influences the village layout and architectural style (Smith 2015). Different climatic conditions require specific architectural forms and material choices, which impact the overall impression of a historical village. The management of water sources also influences the design of main thoroughfares within the village (Jones & Brown 2018).

At the settlement scale, the analysis of architectural aggregations, residential clusters, functional zoning, and the layout of religious buildings is essential. To gain an understanding of the composition of architectural clusters and the overall planning of the village, including the arrangement of residential areas and public spaces, it is crucial to consider the arrangement of residences, such as courtyard-style or row-style. The arrangement of residences reflects the village's social and cultural characteristics. The division of a village into distinct areas for living, working, and public activities helps to maintain a harmonious and functional environment (Johnson 2017, Yang et al. 2020, Jaszczak 2017). The layout and influence of religious buildings and ancestral halls also contribute significantly to the village's character.

At the individual building scale, characteristics such as building types, facades, materials, and structures are considered. The village's historical and functional diversity is reflected in its diverse range of building types, including residential, commercial, warehouse, and public buildings (Gonzalez 2016). Elements such as doors, windows, and roofs significantly influence the village's

aesthetic and architectural style. The use of materials such as wood, stone, and brick affects the village's color palette and visual appeal. In addition, structural forms such as beam-column structures and brick-and-stone structures contribute to the village's architectural integrity. Finally, the temporal hierarchy, including historical evolution, significant events, and building renewal, must be considered. Understanding the village's establishment and development process is crucial (Korten 1980, Li et al. 2019). Historical events such as wars and natural disasters can have a significant impact on the village's architecture. The renovation, expansion, and reconstruction of buildings during different historical periods contribute to the dynamic changes in the village's architectural and streetscape (Li et al. 2019). Therefore, it is essential to record the current architectural features of historical villages accurately and efficiently, and to establish a data library for this purpose.

The Role of Designers in Traditional Village Preservation and Revitalization

Designers play a pivotal role in preserving and revitalizing traditional villages, contributing their expertise in various stages of the process. The complexities involved in balancing cultural preservation with modernization, and the absence of standardized methods for assessing the historical significance of sites can make decision-making challenging for designers (Smith 2018). Despite the existence of evaluation standards or rating systems like the Leadership in Energy and Environmental Design (LEED), the decision-making process for designers remains complex. Efforts to preserve and revitalize historic villages encompass architectural and environmental considerations, cultural heritage, community needs, and economic feasibility. Designers must develop strategies that respect historical and cultural heritage while addressing local realities and future development needs (Gong & Li 2020, Sanchez & Wang 2019). Designers must rely on their experience, intuition, and collaboration with local communities in such contexts to make informed decisions.

Digital Technology Applied in Historical Village Design

The preservation and revitalization of traditional villages have become focal points in cultural heritage preservation, with the aim of improving living conditions while maintaining the characteristic spatial layout of these settlements. Conventional approaches to analyzing historical villages often rely on labor-intensive data collection processes, such as on-site investigations or photographic assessments. However, these methods are costly and often hindered by challenges such as the loss of historical documents, lack of data information, and sampling difficulties due to geographical or topographical factors.

In light of these challenges, growing research has investigated leveraging advanced computer technology to preserve and revitalize historical villages. Digital technologies (Xiao et al. 2018, Sestras et al. 2020) such as mapping, imagery analysis, and 3D modeling have been introduced to preserve and revitalize historic villages for data collection, visualization, analysis, and assessment. For

instance, 3D modeling has been used by Yu et al. (2019) to recreate historical village structures, allowing for detailed virtual tours and aiding in restoration efforts. Similarly, Li et al. (2021) employed imagery technologies to monitor and assess the condition of historical buildings, facilitating proactive maintenance and conservation strategies. By mapping the landscapes and incorporating oblique imagery, Pratt and Heyes (2022) can more effectively comprehend the historical significance of these sites and work toward their preservation. (Zhang et al. 2022) utilized oblique imagery and mapping technologies to effectively encapsulate the traditional settlements and villages' essences to enhance the understanding of traditional villages and revitalize them.

Additionally, parametric design tools have been used for generating complex architectural forms and optimizing design alterations in revitalizing traditional villages. The parametric planning and design method is more creative than the traditional manual planning and design method. It is easier to create a form that contains a rigorous logic of its spatial organization, which is the most essential and core feature of the current traditional village space (Jiang et al. 2023). Parametric design tools not only enhance design efficiency but also bolster precision and adaptability, thereby better addressing the myriad challenges historicak villages encounter in the processes of preservation and revitalization.

In recent decades, Machine Learning (ML) and Artificial Intelligent (AI) have been applied to architecture design, construction, and operation. Among the most prevalent technologies applied to in architecture include natural language processing, computer vision (CV), and neural networks (Sanchez 2023). However, there is comparatively less applications in building planning, especially in rural settings (Hastak and Koo 2017). Due to the pivotal role of visual data, CV assumes particular importance in the planning and design process (Liang et al. 2023), especially in swiftly acquiring the relevant parameters of existing buildings and urban areas. To harness the efficiency advantages of Machine Learning (ML), Artificial Intelligence (AI), and neural networks, computer vision (CV) technology can be applied to various aspects of research and design within historical villages. By leveraging ML, AI, and neural networks, CV can streamline data acquisition processes, aid in the analysis of historical village layouts and streetscapes, and facilitate architectural surveys. This integration enables the automated extraction of relevant information from large datasets, allowing for more accurate and comprehensive assessments of historical contexts. Furthermore, these technologies empower designers by providing valuable insights and supporting informed decision-making throughout the planning and design phases of historical village preservation and revitalization projects.

Despite significant advancements in digital technologies and their applications in heritage conservation, several gaps remain in the effective preservation and revitalization of historical villages. One major gap is the lack of integrated platforms that combine multiple advanced technologies for comprehensive analysis and design. Current methodologies often involve labor-intensive and fragmented approaches that do not fully leverage the potential of emerging technologies like UAV 3D oblique imagery and computer vision (CV). This research addresses these gaps by proposing a novel cross-software evaluation plug-in that integrates

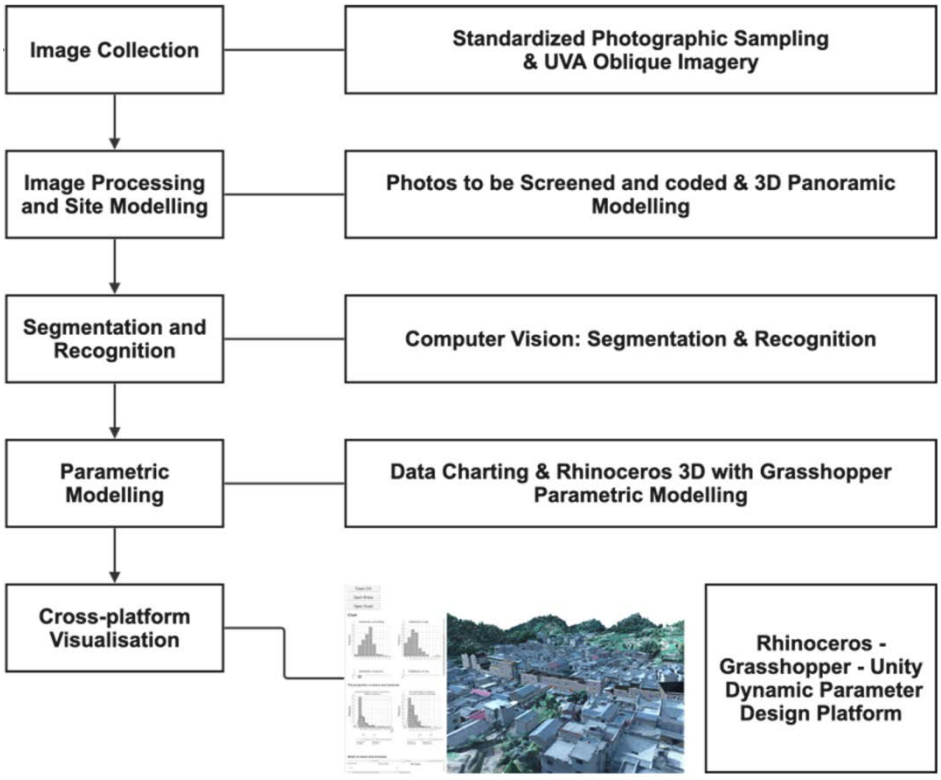
Excel, Rhinoceros-Grasshopper (GH) and Unity 3D. This platform facilitates the parametric analysis, editing and visualization of spatial elements in historical villages, offering a more efficient and economical solution for data collection and design evaluation. The application of this platform in Qinchuan Historical Village, Zhejiang Province, demonstrates its potential to enhance the preservation and revitalization efforts by providing a dynamic and interactive tool for designers and researchers.

Methodology

The Qinchuan historical village in Zhejiang Province, China, is the site of the field study to demonstrate the method/technologies proposed in the study. All data and images were gathered from this location, and the cross-software evaluation plug-in will be illustrated using Qinchuan as a case study.

A five-step process is employed to outline the construction of a cross-software evaluation plug-in for the revitalization of historical villages. These steps include image collection, data processing, segmentation and recognition, parametric modeling, and visualization (see Figure 1).

Figure 1. *The Five-Step Methodology for Creating Cross-Software Evaluation Plug-in*



Source: Made by author.

The data and image materials were collected with great care by our research team. Upon completion of the oblique image, the 3D model is generated using the open-source software GET3D Cluster (GC). The use of CV technology allows for the segmentation and recognition of 10 streetview elements within the image. From there, the figure-occupancy data for each element is determined and a graph of its normal distribution is generated. Subsequently, the 3D model is linked with the parametric design software Grasshopper (GH), which enables parametric adjustments to the proportions of streetview elements in the facade. This ultimately generates a new design. All parameter tuning is conducted via a developed cross-software evaluation plug-in tool.

Image Collection

The initial step in acquiring information about the historical village is the collection of images. A standardized sampling methodology employing oblique imagery is utilized for the photographic documentation.

- Standardized sampling

  Along the main road of the historical village, which measures 980 meters in length, our team captured standardized photographic samples of streetview elements. The camera was positioned on the central axis of the main road, with images captured at 10-meter intervals. Each group of images included both forward and backward perspectives.

  For this process, a Canon 60D camera and SIGMA ZOOM 18-200mm 1:3.5-6.3 II lens were employed, maintaining a camera height of 170 cm ± 2.5 cm and a horizontal angle to the ground of ± 5 degrees. The focal length employed was within the range of human eyes, equivalent to a lens of 18mm, which is equivalent to a focal length of 28.8mm.

  The standardized photography was conducted over two days, from 2:00 p.m. to 4:00 p.m. each day, resulting in the capture of 194 images. The image data obtained from this standardized photography will be integrated into the historical village dataset, serving as the basis for segmentation and recognition and subsequently acting as references for parametric design.

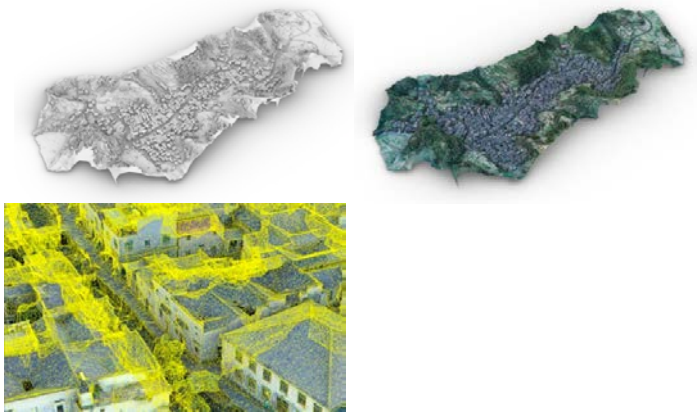
- Oblique imagery

  Oblique Imagery employs DJI-Terra for shooting. Initially, the village was. manually demarcated based on Google Maps, and five flight paths were created in the format of path files (kml). These paths were then imported into the UAV equipment, resulting in the capture of 2192 photos. All images are utilized to create a dataset, facilitating the generation of 3D models for historical villages. Firstly, the flight range and geographic location information of the UAV must be determined through Google Maps, and a KML geographic location information file must be generated.

  Secondly, the KML geographic location information file must be imported into the DJI Phantom 4 RTK mission manager, the appropriate flight altitude and mission settings must be debugged, and the flight path

information for 5-direction tilt-shot photography must be generated.
Thirdly, the flight path and photography parameter information is uploaded to the drone, the appropriate take-off and landing sites for the UAV are identified, and the flight photography mission is initiated.
Once the mission has been completed, the data generated by the tilt-shot photography will be processed. This data will be uploaded to an open-source software, GET3Dcluster, which is designed to combine the mission KML file with the image database.
The data will then be encoded and sorted automatically into a cloud file, which will generate a 3D spatial point cloud based on the image information. This will then be converted into a spatial mesh file through the use of cloud computing, which will automatically generate the mesh file with material and color information. The 3D spatial information of historical villages can be generated with material and color information, which can then be edited using a mesh file or Objective file.

Figure 2. *3D Spatial Information - Spatial Material and Color Information - Editable Mesh Grid*



Source: Made by author.

Image Processing and Site Modeling

The combination of the aforementioned two shooting methods results in the creation of the historical village dataset, in which the collected image data and data jointly contribute to its formation. The initial processing of the dataset involves a cleaning procedure, during which the images captured through standardized sampling are manually screened to remove any images that have been overexposed or out of focus. Subsequently, the images are encoded. The photos captured through standardized sampling are manually encoded, whereas those taken through oblique imagery undergo automatic encoding during the shooting process.

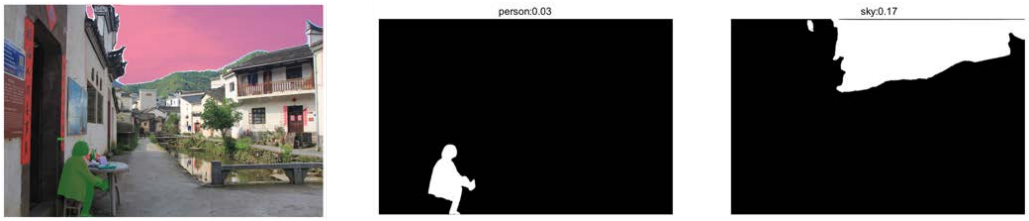
The images captured along the five flight paths are imported into the open-source software GET3DCluster, utilizing cloud-based automatic modeling software in accordance with the coding order. This process generates a private cloud project that, upon cloud processing, automatically produces a 3D historical village panoramic model along with associated materials based on the input pictures.

Segmentation and Recognition

Semantic segmentation and recognition are both essential scenarios of CV applications (Chai et al. 2021). DINO (Liu et al. 2023) classifies all elements into ten categories-building, sky, ground, tree, door, window, water, plants, person, and transportation-by object detection in a preconfigured scale and ratio calculation. Semantic-SAM (Li et al. 2023) is used to segment photographs taken under harmonized standards into elements. The integration of models enables automatic image processing and analysis, allowing batch processing of image files, identification and segmentation of different objects within the images, and recording the pixel ratio for each category. The specific workflow is as follows:

First, set the environment and path to get the working directory for the 194 photos. Set the path for the GroundingDINO and SAM model weight files and check for their existence. After importing the necessary libraries and modules and determining the device type, load the GroundingDINO and SAM models. After traversing the data directory, identification and segmentation are performed for each file. The process begins by reading a single image file, using the GroundingDINO model to detect a specific streetview element in the image, annotating the detected object, and drawing bounding boxes and labels. The SAM model is then used to segment the detected target and create a mask. At the same time, the segmentation results and category labels are applied to the original image. Further data analysis is then performed by calculating the pixel proportion of each segmentation mask, generating a proportion list for each category, and summarizing the proportion of all categories for each image (see Figure 2). To ensure the accuracy of recognition, a cyclic processing concept is introduced. This entails recognizing, segmenting, processing, and summarizing each element in the 194 image files in the directory. Finally, the pixel ratio data for the ten streetview elements in each image file is obtained.

Figure 2. *Semantic Segmentation and recognition of Element and its Ratio for Each Category*



Source: Made by author.

Parametric Modeling

Grasshopper (GH), a parametric design plug-in of Rhinoceros, is used for parametric adjustment to design the renovation of historical village buildings (see Figure 3).

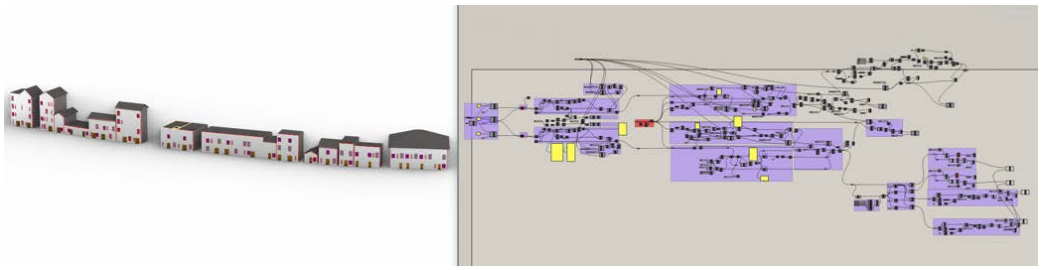
Excel data is imported into GH, and the proportion data for doors and windows, S-door/S-wall total, and S-window/S-wall total for Qinchuan Historical

Village are extracted. The proportion data for doors and windows are then organized by size, and the maximum and minimum values for each group interval are determined. Equal partitions corresponding to the number of facades are created, with the proportion of doors and windows associated with each interval. The number of data within each interval is calculated. The median value of each interval is selected and replicated a certain number of times, resulting in 194 data groups consisting of 27 different data points.

Select the facade contour using a curve and arrange it from left to right. After obtaining the door width by dividing the door/façade area of the buildings along the street and applying the door height module, it is aligned with a fixed module to ensure that it adheres to standard door width sizes. The positioning points for the doors are determined by dividing the bottom edge of the facade and randomly selecting a specific point to place the door.

The facade contour line is selected using a curve to assess the facade height and determine if the window is multi-layered. Different layer heights are set at intervals, each with its own layer height line. The iso-layer height lines determine the window positions and are constrained within the facade. By using random height times random width, multiple sets of window sizes are derived. The number of windows inside is determined by checking that the sequentially added area remains within the window ratio. Consequently, window contours of random size are generated and extended at points along the floor height line.

Figure 3. *GH as a Parametric Design Plug-in of Rhinoceros*



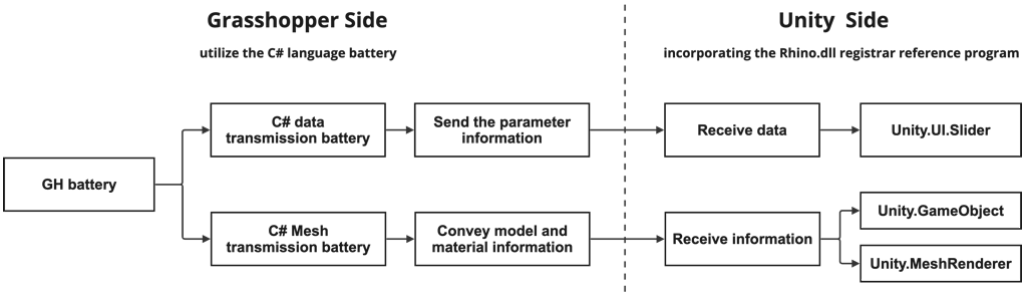
Source: Made by author.

The Cross-Software Evaluation Plug-in

The objective of the cross-software evaluation plug-in is to facilitate visualisation. The software was developed using Unity, a game development software known for its robust code compatibility (see Figure 4). Both Unity and GH employ the C# programming language. To facilitate communication between the two, the Rhino.dll registrar reference program can be incorporated into Unity as a port. Two digital batteries facilitate the transmission of GH data, with the C# Mesh data transmission battery conveying model and material information. Upon receipt of the information, the Unity terminal creates a Unity.GameObject instance, which simultaneously synchronizes the model information and the Unity.MeshRenderer and renders the materials. Once the C# data transmission battery has transmitted the requisite parameter information to the Unity end, a Unity.UI.Slider instance is generated in order to synchronize the parameter

information. The cross-software evaluation plug-in interface displays a three-dimensional model of the street and graphics representing ten elements. The interface permits the user to adjust parameters such as the proportion of doors and windows. Consequently, the 3D model of the street is updated in real-time in accordance with the specified parameters, facilitating the rapid generation of revised design schemes.

Figure 4. *GH Conveys Data and Information to Unity*

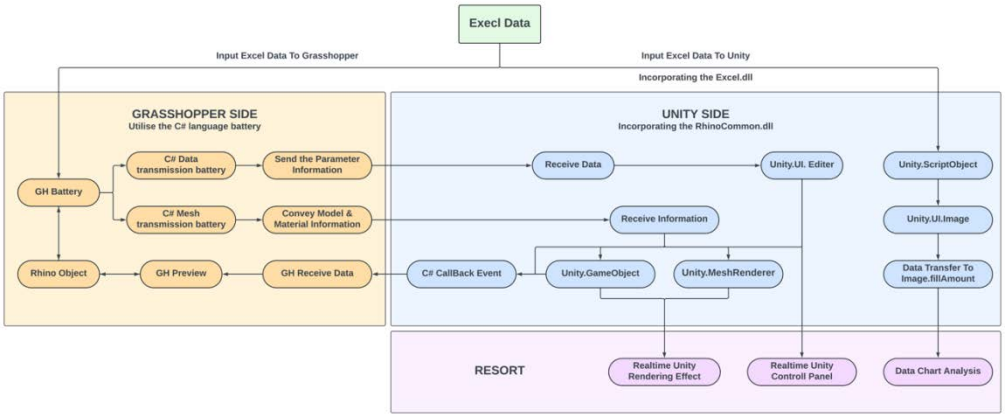


Source: Made by author.

Results

The cross-software evaluation plug-in is a *Data-Rhinoceros&GH-Unity* interactive visualization interface. Using the button assist, all the data of the streetview elements in the Excel file are imported into GH and Unity to obtain the parametric facades, diagrams, and rendered 3D model. By dragging the sliders, the dashboard presents the visualized design results in real time (see Figure 5).

Figure 5. *The Framework of Data-Rhinoceros&GH-Unity Evaluation Plug-in*



Source: Made by author.

Automatic Data Capture and Data Chart Presentation

The data in Excel is subjected to CV segmentation, representing the area ratio of the 10 streetview elements obtained after recognition in the photo. Through coding, we incorporate the Excel.dll library file into Unity as a reference, enabling

Unity to automatically extract horizontal and vertical coordinate data from Excel. This process facilitates the construction of the dataset for Qinchuan Historical Village. The entire dataset is stored in Unity's newly created ScriptableGameObject, which serves as a reference for rendering the data graph.

The data chart is intended to further visualize the data automatically captured in the dataset, focusing primarily on the normal distribution of the 10 streetview elements. Through coding, the maximum value is determined, the horizontal axis is synchronized, and the frequency of data falling within the range is counted. The segmented data is then filled using the Image component in Unity to achieve the visualization of a dynamic data chart.

This allows designers to consider and analyze various environmental and architectural factors in a convenient manner, as well as to gain an intuitive understanding of the statistical and analytical aspects of the street scene. Synchronization enhances the designer's comprehension of the current state of the building, providing guidance for subsequent designs through data charts.

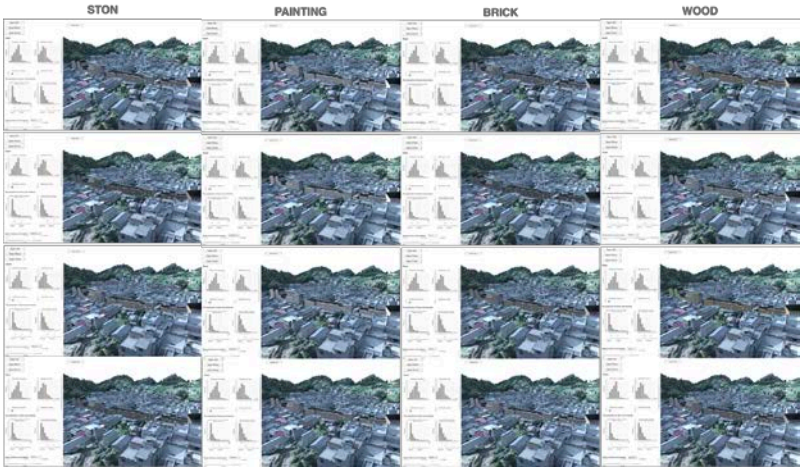
Fine-tune the Proportion Parameters for Streetview Elements in the Design

In Unity, the first step is to create a grid and a general material. It then calls the grid and material from the GH data structure datatree, creating a new list to store the data. This data is synchronized with the new Rhino Runtime event, and the color and transparency information of the material and model is transferred using the GH C# Mesh data transfer component. Unity receives the mesh information using the GeString method and creates a Unity.GameObject instance to generate a 3D facade model. At the same time, material rendering information is passed from GH to Unity via the C# Mesh component, resulting in the creation of a Unity.MeshRenderer instance that represents the facade rendering effect.

The Unity side receives information from the slider and generates a Unity.UI.Slider instance, allowing users to adjust parameters by dragging the slider left and right. When the normal distribution plot is within the threshold range, users can not only adjust the proportions of doors and windows to buildings separately, but also fine-tune details such as windowsill height, window thickness, and door frame thickness. By adjusting the Random Seed value, users can achieve a randomized distribution of doors and windows.

Given the significant impact of building materials and colors on the preservation and revitalization process, the Unity.UI interface includes a material selection menu. This feature allows users to replace materials on street facades and to select and edit different colors for the same material, further optimizing the streetview facade design (see Figure 6).

Figure 6. *User Interface (UI) for Cross-Software Evaluation and Editing of Façade: Streetview Elements*

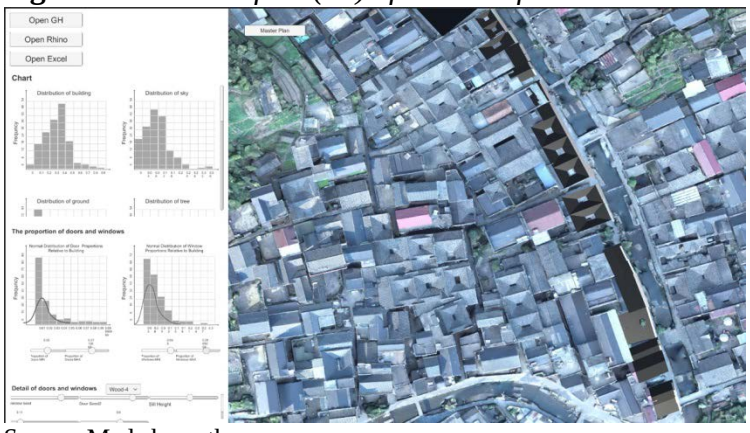


Source: Made by author.

Dynamic 3D Model Rendering

In Unity, the initial step involves the establishment of a grid and the general material. This is then called from the GH data structure datatree, creating a new list to store the data. This data is synchronized with the new Rhino Runtime Event, and the color and transparency information of the material and model is transmitted through the GH C# Mesh data transmission component. Unity receives the mesh information using the GeString method and creates a Unity.GameObject instance, generating a 3D facade model. Simultaneously, material rendering information is transmitted from GH to Unity through the C# Mesh component, resulting in the generation of a Unity.MeshRenderer instance, representing the facade rendering effect. The interface includes a "Master Plan" button, which generates real-time rendered images of the desired design area from an overhead perspective. It provides an overhead view of the buildings within the design area, including the site environment, settlement relationships, hydrological conditions, and vegetation (see Figure 7).

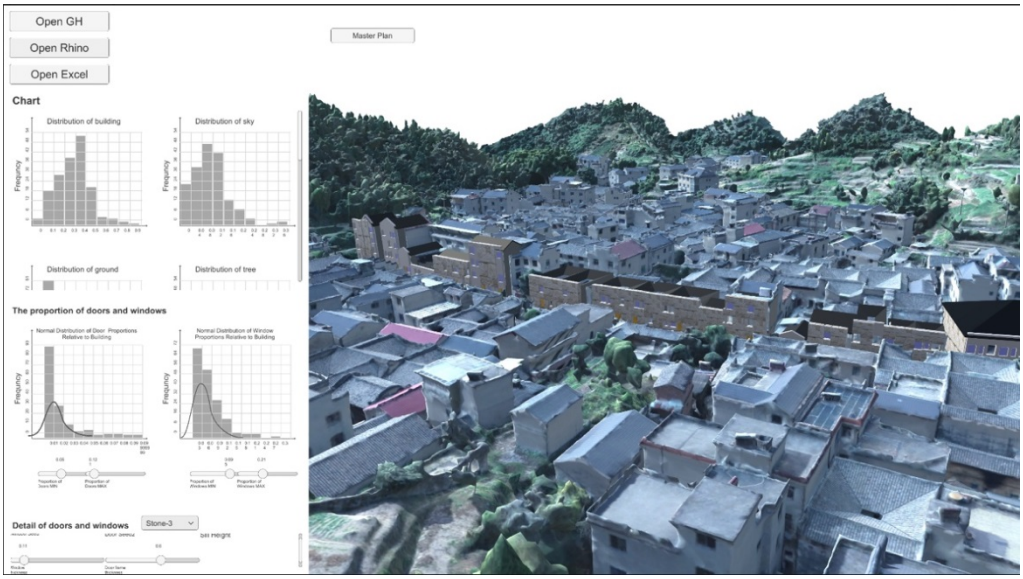
Figure 7. *User Interface (UI) of Cross-Software Evaluation Plug-in*



Source: Made by author.

The Unity.UI interface allows users to control the real-time 3D rendering interface using the mouse and scroll wheel. This enables the generation of real-time 3D rendered models from any desired angle based on user requirements (see Figure 8).

Figure 8. *User Interface (UI) of Cross-Software Evaluation Plug-in*



Source: Made by author.

The 3D model undergoes dynamic changes in response to adjustments to certain parameters, and the results of these adjustments can be observed in an intuitive manner. The integration of real-time data changes into the design workflow allows for instantaneous model updates, significantly enhancing design efficiency.

Discussion

Using the method described in Section 2, we developed a dataset for the historical city of Qinchuan, including streetview elements along the main road and 3D model data for the entire city. Using CV technology, the main roads were segmented and identified based on the 10 streetview elements, and the proportions of these elements were further analyzed. Systematic data collection and data chart analysis for the street scene elements of historical villages can help design staff provide clearer insights and analytical data for the influencing factors of Streetview. Within the threshold range, the proportions of doors, windows and buildings are parameterized and adjusted according to the normal distribution chart, effectively facilitating the renewal and design of street facades for historical buildings. As a cross-software evaluation plug-in breaks down the barriers between software and enables cross-software collaborative design, thereby increasing design efficiency.

However, this experiment identified some potential subtle limitations, mainly

concentrated in the early stages of image collection. The photos were not taken during all four seasons, and trees may block houses in summer, a challenge that can be better addressed in future experiments. The transformation of a small number of houses has slightly compromised the unity of opposites and heights. In the future, more accurate and faster streetview data and base parameters can be achieved through advanced and efficient streetview data collection tools and technologies. Targeted CV training in old village streetscapes can further improve recognition accuracy.

This study revealed several shortcomings and limitations in our existing data collection methods, namely standardized photography and drone oblique imagery. Issues such as blind spots, object occlusion, and shadows were identified. Additionally, there are limitations in the comprehensiveness of the data, as it lacks interior spatial information of individual buildings and high-resolution scans of specific historical features. Therefore, to upgrade our spatial 3D database in the future and make the plug-in more systematic, efficient, and precise, it is necessary to integrate more professional, accurate, and efficient technical measures.

Conclusion

The preservation and revitalization of historical villages is a complex undertaking that involves numerous factors, including historical context, cultural heritage, local characteristics, and cultural heritage protection. This makes it a challenging and lengthy endeavor. Consequently, the integration and development of new design tools that utilize CAAD and AI technologies become crucial. Currently, the methodologies employed for updating historical villages are relatively antiquated, and the majority of existing technologies are disparate, lacking cohesion and exhibiting low design efficiency.

This paper outlines the development process of the cross-software evaluation plug-in, which efficiently imports analysis data of street view elements through CV at the initial stage. This establishes cross-software linkage, connecting an Excel database to Rhinoceros-GH-Unity. The cross-software evaluation plug-in employs a parametric dynamic adjustment process through user interface (UI) functionality, which in turn displays the corresponding 3D model results in real-time. The dashboard can assist decision-makers and stakeholder groups involved in the protection and renewal of historical villages, thereby enhancing the efficiency of early conceptual design. Moreover, the tool has broader applicability as a design tool across various fields, guiding designers to conduct more scientific and efficient design work.

Balancing historical preservation with modern development is a core issue for the future development of historical villages (Labadi & Logan 2015). To address this, it is crucial to provide designers and researchers with more freedom and intuitive tools to operate dynamic 3D renderings. This would enable them to better analyze, design, and study the historical landscape, architectural changes, and renovation directions of historical villages.

By integrating advanced 3D visualization technologies and enhancing the user

interface of the cross-software evaluation plug-in, which offers a more intuitive and interactive experience. This will empower designers and researchers to seamlessly manipulate 3D models, visualize potential changes, and make informed decisions about preserving historical features while accommodating modern needs.

Furthermore, developing a comparable platform for designers will facilitate collaborative efforts, ensuring that all stakeholders can contribute to the sustainable and balanced development of historical villages. By leveraging these advancements, we can create a more holistic approach to heritage conservation and modernization, preserving the unique cultural identity of historical villages while fostering their growth and development.

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